On-Chip Noise Sensor for Integrated Circuit Susceptibility Investigations

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***Abstract*—With the growing concerns about electromagnetic compatibility of integrated circuits, the need for accurate prediction tools and models to reduce risks of noncompliance becomes critical for circuit designers. However, an on-chip characterization of noise is still necessary for model validation and design optimization. Although different on-chip measurement solutions have been proposed for emission issue characterization, no on-chip measurement methods have been proposed to address the susceptibility issues. This paper presents an on-chip noise sensor dedicated to the study of circuit susceptibility to electromagnetic interferences. A demonstration of the sensor measurement performances and benefits is proposed through a study of the susceptibility of a digital core to conducted interferences. Sensor measurements ensure a better characterization of actual coupling of interferences within the circuit and a diagnosis of failure origins.**

***Index Terms*—Electromagnetic compatibility (EMC), integrated circuits (ICs), interference measurement, on-chip sensor, susceptibility testing.**

I. Introduction

THESE LAST years, the concerns about electromagnetic compatibility (EMC) of integrated circuits (IC; emission and susceptibility issues) have grown considerably. The need for prediction of noncompliance risks during the design stage has become critical for IC manufacturers in order to reduce redesign costs and time to market [1]. Although several tools and prediction methodologies have been developed recently [2], [3], accurate measurements of on-chip noise are still critical information for designers for model validation and design optimization.

The external characterization of fast transient current induced by circuit activity is limited by the bandwidth of CMOS analog buffer and electrical parasitic elements of chip and package interconnects. Numerous on-chip measurement devices have been proposed over the last 15 years, and published results have demonstrated the positive contribution of on-chip measurements to characterize accurately and solve power integrity, simultaneous switching noise, ground bounce, crosstalk, or substrate coupling issues. The different systems for on-chip noise characterization can be classified into two families: the on-chip waveform capturing circuits and the noise detectors. Most on-chip waveform capturing circuits are based on a subsampling cell [4], [5] dedicated to repetitive signal measurements with very small time resolution, comprised between 100 ps [6] and 10 ps [7], [8]. Despite excellent time resolution characteristics, the circuit under test must operate in a special mode where a periodic event is generated, so the noise produced during normal operating mode cannot be characterized. In [9], the use of two subsampling cells allows the extraction of the signal autocorrelation and, thus, its power spectral density without requiring repetitive chip operations. Noise waveforms can also be measured by built-in probing techniques which rely on small voltage-to-current converter cells [10] and can be distributed over IC power distribution networks (PDNs) to obtain a noise distribution map [11]. The second category, i.e., the noise detectors, aims at providing the primary characteristics of noise without acquiring the timing waveform. Their advantage lies in the reduced amount of data to process to obtain information about on-chip noise. In [12], an on-die droop detector is presented. Amplitude, duration, and polarity of power supply fluctuations are characterized in real time by comparing signals to programmable thresholds. Only significant events are characterized by the noise detector which transmits 1 b per acquisition.

However, although on-chip noise measurement techniques have been used for power integrity and conducted emission characterization in digital ICs, they have never been used for the characterization of susceptibility to electromagnetic interferences (EMIs). Susceptibility of ICs has become one of the major issues for all circuit classes (digital, analog, RF, and power). Concerns about failure mechanisms, EMI coupling, and susceptibility modeling at circuit level have arisen recently [13]. The main problem for IC designers is to be able to evaluate the compliance according to standard susceptibility tests prior to circuit fabrication. The susceptibility of a circuit depends not only on the intrinsic sensitivity of disturbed functions to EMI-induced voltage fluctuations but also on the filtering effect of package bonding wires, chip interconnects, on-chip decoupling, substrate coupling, etc.

In this context, measuring the amount of EMI-induced noise on a sensitive node of a circuit is critical for IC designers for two reasons. First, an accurate measurement of parasitic voltage fluctuations on circuit terminals helps to determine the actual

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sensitivity of the disturbed function. Thus, if this measurement confirms that a susceptibility peak is linked to an efficient coupling of the EMI within the circuit, designers should try to enhance the filtering effect of the circuit at this particular frequency (e.g., by adjusting on-chip decoupling capacitance value). Second, comparing measurements to simulation results can help to validate circuit susceptibility models.

This paper aims at presenting an on-chip sensor dedicated to the characterization of the EMI-induced noise during standard immunity tests and demonstrating through a case study how it can be helpful in solving susceptibility issues. Section II presents briefly a state of the art of standard methods for IC susceptibility characterization. Their limitations in precisely extracting the actual susceptibility level of a circuit compared to an on-chip measurement are explained, and the general requirements of an on-chip noise sensor for IC susceptibility characterization are introduced. In Section III, the acquisition technique and the sensor architecture are presented. Section IV describes the sensor design and the experimental characterization of sensor performances. In Section V, the sensor is used to study the susceptibility of a digital core to conducted EMI experimentally.

II. Measurement of EMI-Induced Noise for IC Susceptibility Characterization

A. IC Susceptibility Characterization

Susceptibility tests aim at characterizing sensitivity level of electronic equipment to conducted or radiated EMIs and ensuring the compliance to limits defined by standards or customer requirements. Susceptibility test setup definitions and recommendations are given by standards such as CISPR 25 [14]. The susceptibility of equipment depends not only on numerous parameters, e.g., shielding effectiveness, printed circuit board (PCB) routing, decoupling, filtering, etc., but also on circuit susceptibility. Thus, EMC requirements at equipment level are laid down for ICs. IC manufacturers are forced to qualify the susceptibility of their devices and ensure the compliance with customer requirements.

Specific standards have been defined to test the susceptibility of IC, such as IEC 62132 [15]. This standard widely used by IC manufacturers proposes different types of tests to characterize IC sensitivity to conducted or radiated EMI up to 1 GHz. For diagnosis purposes and precompliance tests, IC manufacturers usually use the IEC 62132-4—direct power injection (DPI) method [16], based on conducted EMI injections applied on one or several pins.

B. Limitation of External Characterization of IC Susceptibility

Immunity test methods defined by IEC 62132 give indications about the IC behavior exposed to RF disturbances by an external observation of voltage or current waveforms. The propagation of the RF interference through package and circuit interconnects, its penetration efficiency, and the coupling path dependence on frequency remain unknown. Moreover, the actual immunity level of the circuit, i.e., the required voltage fluctuation magnitude applied across circuit terminals to induce a failure, is not evaluated.

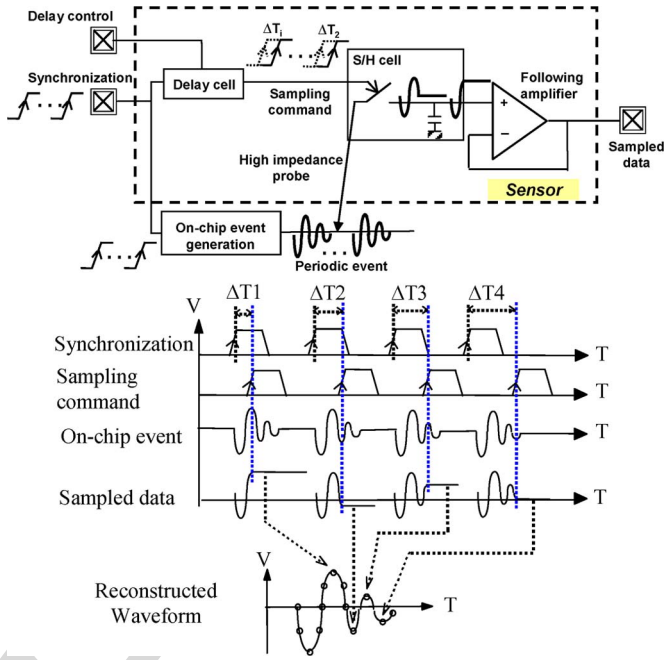

Fig. 1. Original synchronous on-chip noise sensor architecture and sequential equivalent-time sampling principle [17].

Due to the filtering effect of package, circuit interconnects, and bandwidth limitation of output buffers, off-chip measurement fails to provide accurate characterization of EMI-induced noise within circuits over several tens of megahertz. The accurate characterization of the actual susceptibility level of a circuit relies on a low intrusive and wideband on-chip measurement of EMI-induced voltage, i.e., at least the frequency range specified by IEC 62132 (150 kHz–1 GHz). The sensor must measure the voltage amplitude of EMI-induced noise across all types of nodes and withstand electrical overstress without large variations of its performances. Parasitic couplings with other blocks of the circuit must be reduced to prevent from disturbances of measurement. Moreover, the sensor must occupy a small area and a reduced I/O number to simplify its insertion in an existing design.

III. On-chip Noise Sensor Description

A. Synchronous On-Chip Noise Sensor

A first version of the on-chip noise sensor was designed in the early 2000s to address signal and power integrity issues at circuit level [17], [18]. The sensor is based on a sequential equivalent-time sampling [19]. Its architecture and the principle of signal reconstruction are described in Fig. 1.

An on-chip sample and hold (S/H) circuit directly probes the voltage along the circuit interconnects and operates in subsampling conditions. The probe input impedance is large enough to ensure a noninvasive measurement. The signal acquisition is made over several occurrences of a reproducible phenomenon, and only one sample is taken at each repetition. An external synchronization signal is used to trigger off the on-chip event

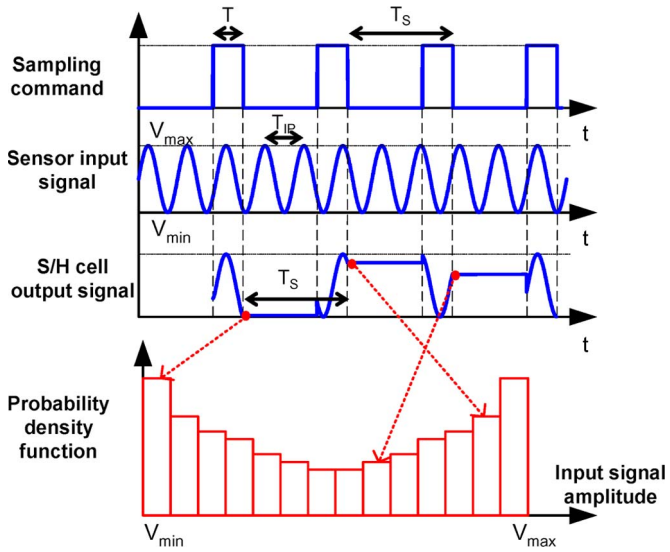

Fig. 2. Asynchronous sampling of a signal and extraction of pdf of the signal amplitude.

to both characterize and activate the S/H cell. The sampling command is shifted from the synchronization signal by a delay cell. The time resolution of the reconstructed waveform is set by the minimum delay step, while its duration is set by the maximum delay produced by the delay cell. Samples are externally stored for waveform reconstruction. A very high virtual sample rate can be reached without severe constraints on hardware bandwidth.

B. Asynchronous On-Chip Noise Sensor

The reconstruction of EMI-induced noise waveform based on sequential equivalent time is difficult. By definition, the EMI characteristics are unknown (amplitude, frequency, and waveform). Waveform reconstruction of the EMI-induced noise relies on acquisitions triggered on a repeatable external interference, which is possible only if the characteristics of the interference are known in advance. However, this condition is usually not ensured, so the signal is sampled at random instants and the waveform cannot be reconstructed.

Nevertheless, even if the sampling cannot be synchronized with the interference, an asynchronous or random sampling can provide valuable information about EMI-induced noise properties. The proposed sensor reuses the same architecture but operates in an asynchronous sampling mode. The S/H cell and the output amplifier are kept, but the delay cell is removed. A low-frequency trigger commands the S/H cell to randomly subsample the input signal. The value stored at the S/H cell output is a random variable which constitutes the outcome of the instantaneous amplitude of input signal measurement. As explained in Fig. 2, this random acquisition allows the extraction of signal amplitude probability density function (pdf) [20]. The pdf provides the likelihood of the input signal having a given amplitude at any time. Whatever the input signal frequency, the pdf of the signal amplitude can be correctly extracted provided that the S/H cell or the output amplifier does not distort or filter the sampled signal.

This acquisition mode can provide valuable information about circuit susceptibility. First, for a given type of disturbance, the average amplitude of the EMI-induced noise can be extracted from the signal amplitude pdf. Moreover, for large-amplitude-disturbance injection, changes in amplitude pdf shape suggest that some distortions induced by the circuit (e.g., electrostatic discharge (ESD) clamp devices triggered by large disturbances) affect the signal.

IV. Sensor Design and Characterization

A. Test Chip Description

The asynchronous on-chip noise sensor has been implemented in a 0.25-μm SMARTMOS 8 technology test chip from Freescale Semiconductor. This technology aims at designing digital and high-voltage (HV) analog mixed circuit that can withstand voltages up to 80 V. The test chip is dedicated to the susceptibility characterization of various analog and digital structures. Ten on-chip sensors have been implemented to monitor power supply voltage fluctuation as close as possible to each block. Moreover, three different sensors have been duplicated for calibration purpose.

B. Design of the On-Chip Noise Sensor

General Architecture: Fig. 3 shows the architecture of the on-chip noise sensor. The sensor is made of three main elements: an attenuator, an S/H cell which operates in subsampling mode, and an output amplifier. The attenuator and the S/H cell form a high-impedance probe which ensures a low intrusive voltage measurement. Three sensor versions have been designed to measure voltage fluctuation in the different power supply domains of the circuit (2.5, 5, and 12 V): low-voltage (LV) range (0–3.75 V), medium-voltage (MV) range (0–7.5 V), and HV range (0–40 V) versions. They are based on the same architecture and use the same S/H cell and operational amplifier. They only differ from the attenuator ratio of the input attenuator. Table I gives the characteristics in terms of voltage range and the gain of the different parts of the three sensor versions.

The sensor response is sensitive to voltage fluctuations coupled on its power supply and its substrate reference. The isolation of the sensor to external disturbances and to noise produced by the other blocks of the circuit is a critical requirement. Thus, the output amplifier and sensor input–output (I/O) are supplied by an external and dedicated 5-V power supply. At board level, this power supply is separated and carefully decoupled. The S/H cell and the amplifier input stage are supplied by a quiet 2.5-V power supply provided by an internal built-in voltage regulator and powered by the 5-V sensor power supply. To prevent from interference coupling on the sensor by the substrate, all the devices of the sensor are isolated from the P substrate by a buried n-layer and dielectric-filled trenches on the sides.

Attenuator Design: The attenuator and the S/H cell are the most critical parts of the sensor to ensure a large bandwidth, improve the linearity, and reduce the voltage dependence. They

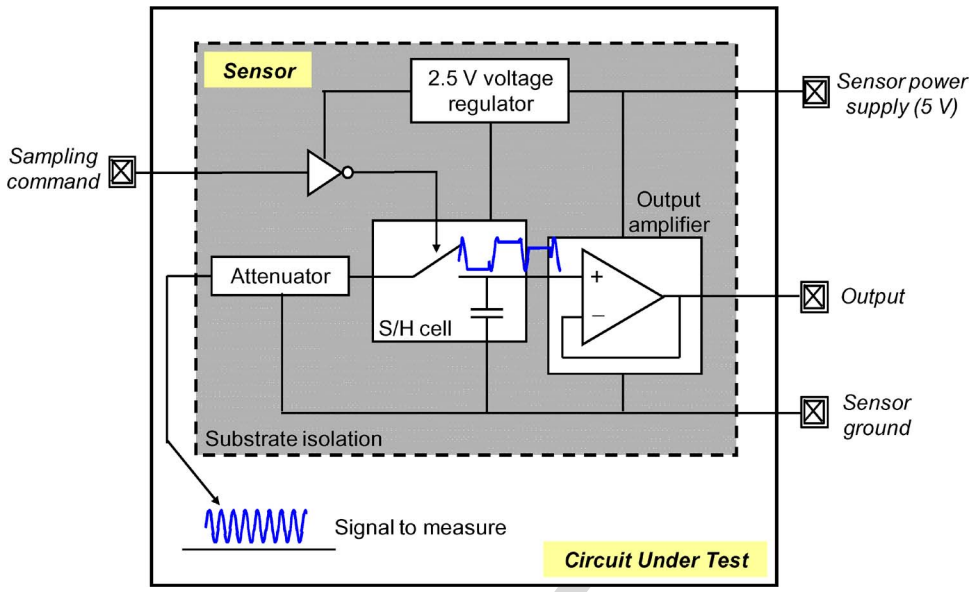

Fig. 3. Asynchronous on-chip noise sensor architecture.

TABLE I
CHARACTERISTICS OF THE THREE SENSOR VERSIONS

Sensor version	Input signal range	Attenuator ratio	Amplifier gain	Output range
Low voltage	0 to 3.75 V	2/3	2	0 to 5 V
Medium voltage	0 to 7.5 V	1/3	2	0 to 5 V
High voltage	0 to 40 V	1/16	2	0 to 5 V

are made of isolated LV transistors to prevent the impact of external disturbance and reach a 2-GHz bandwidth. Fig. 4 shows the electrical schematic of the attenuator and the S/H cell with parasitic elements.

The attenuator is based on a resistive voltage divider made of polysilicon resistor. Polysilicon resistors are designed above thick oxide to withstand voltage up to 80 V. Polysilicon capacitors C_1 and C_2 are added to compensate the parasitic capacitance of the resistors (C_{R1} and C_{R2}) and maintain a flat frequency response. The expression of the transfer function $K(\omega)$ of the attenuator is given by

$$K(\omega) = \frac{R_2}{R_1 + R_2} \frac{1 + jR_1(C_1 + C_{R1})\omega}{1 + j\frac{R_1 R_2}{R_1 + R_2}(C_1 + C_{R1} + C_2 + C_{R2})\omega} \quad (1)$$

The compensation capacitance values are chosen according to

$$C_1 + C_{R1} = \frac{R_2}{R_1}(C_2 + C_{R2}). \quad (2)$$

in order to make the pole and the zero of $K(\omega)$ equal.

The values of resistors, and parasitic and compensation capacitors of the attenuators are reported in Table II. The input impedance of the attenuator is larger than 500 Ω up to 2 GHz for the three sensor versions, which is large enough to ensure a noninvasive voltage measurement.

S/H Cell Design: The S/H cell is composed of a transmission gate switch and a storage node composed of parasitic capacitors of the switch, input capacitor of the amplifier, and the storage capacitor. The sizes of the transmission gate transistors are carefully chosen to optimize the bandwidth and reduce the voltage dependence of the ON-state resistance. However, when the S/H cell turns off, a charge injection in the parasitic capacitances between the control signal and the storage node arises. A parasitic offset can be induced on the output voltage. Despite a reduction of the bandwidth, this effect can be reduced by increasing the storage capacitor. Moreover, adding a dummy transmission gate can help to compensate the charge injection effect.

Output Amplifier Design: An analog output signal is driven off the chip, externally stored, and processed by a digital acquisition card. An on-chip analog-to-digital converter could prevent noise coupling on the sensor output signal, but it also increases the sensor size and the number of I/Os. This integration gain comes with special cares in terms of cable shielding, grounding, and output signal processing. As the S/H cell output signal is constant, the noise can be filtered by averaging several samples. Moreover, as sensor I/O shares the same power supply than output amplifier, the sampling command can induce switching noise along this power supply. The sampling of the sensor output signal has to be done far from sampling command transitions.

The output amplifier is a noninverting CMOS amplifier with a gain of two, made of a 2.5-V rail-to-rail input stage and a 5-V AB class output stage. The output stage has been optimized to keep a constant gain of up to 2.5 MHz and reduce parasitic offset and stability issues. The bandwidth of the output amplifier does not affect the sensor bandwidth since the amplifier does not process the sensor input signal, but the S/H output signal. However, the sampling frequency has to be smaller than the amplifier cutoff frequency to prevent the filtering of the sampling signal, which can affect the measured pdf.

On-Chip Sensor Overall Design: The size of the complete sensor in CMOS 0.25 μm is about 200 μm per 300 μm. Table III gives the size of the different sensor parts. A large part of the sensor is occupied by the output amplifier and the voltage

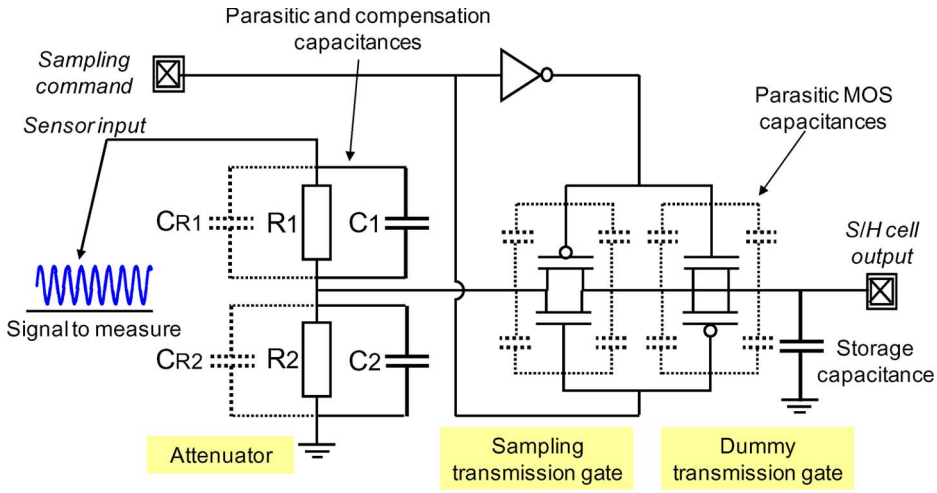

Fig. 4. Schematic of the attenuator and the S/H cell.

TABLE II
CHARACTERISTICS OF ATTENUATOR FOR THE THREE SENSOR VERSIONS

Sensor version	R1 (Ω)	R2 (Ω)	CR1 (F)	CR2 (F)	C1 (F)	C2 (F)
Low voltage	2480	4950	18 f	36 f	400 f	200 f
Medium voltage	9900	4950	71 f	36 f	50 f	200 f
High voltage	38700	2580	16 f	1.1 f	115 f	2 p

TABLE III
CMOS 0.25-μm SENSOR SURFACE

	Width x Length (μm)
Output amplifier	280 x 120
Voltage regulator	270 x 80
Attenuator and S/H cell	20 x 200
Sensor surface	300 x 200

regulator. The total surface of all the sensors of the circuit could be reduced if the output amplifier and the voltage regulator are shared by all the sensors and the outputs of all S/H cells are multiplexed on the common output amplifier.

C. Characterization of the Sensor

In this part, the complete characterization of the sensor performances (I/O characteristic, transfer function, sensitivity to temperature, and aging) is presented. The characterization of the sensor is necessary to calibrate the sensor, i.e., compensate the nonideal behavior of the sensor.

1) Sensor Calibration Procedure: The sensor operation is affected by imperfections and mismatch in the implementation of its elements, which degrades the output responses. The output amplifier is not perfectly linear, so the gain is not constant. Moreover, errors in attenuator resistance values can change the gain of the sensor. Moreover, both the amplifier and the parasitic capacitance of the S/H cell produce an offset voltage. The I/O characteristic is measured to check the sensor linearity and then calibrate the sensor. It consists in applying a constant and known voltage on the sensor input and measuring the voltage amplitude of the output samples. A linear relation

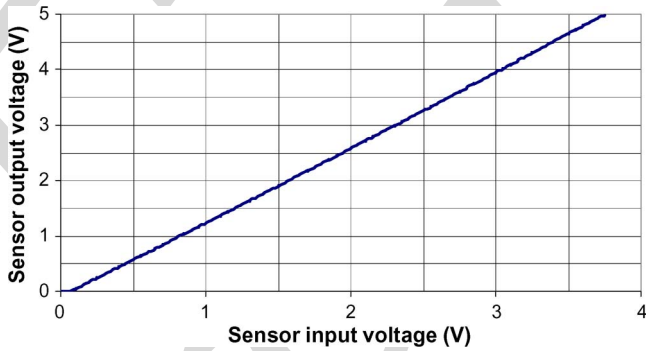

Fig. 5. LV sensor I/O characteristic.

TABLE IV
SENSOR GAIN AND OFFSET CHARACTERIZATION

Sensor version	Theoretical gain	Measured gain	Measured offset
Low voltage	1.333	1.353	100 mV
Medium voltage	0.667	0.677	1 mV
High voltage	0.125	0.134	3 mV

can be established between sensor output and input. From this relation, both static gain and offset can be extracted to compensate sensor imperfections. The LV sensor is highly linear above 0.15 V, as shown in Fig. 5. The MV and HV sensors are also linear above 0.3 V and between 3 and 37 V, respectively. The measured gain and offset for the three sensor versions are reported in Table IV.

2) Accuracy of Sensor Measurements: The I/O characteristic shown in Fig. 5 makes the link between the actual and the measured voltage levels and compensates the systematic errors due to sensor imperfections. However, this characterization and the measurement repeatability are disturbed by random errors

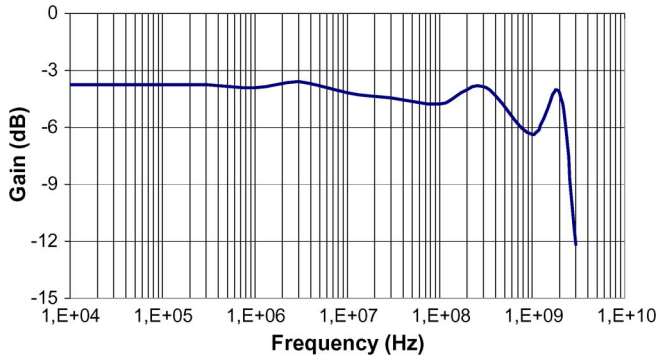

Fig. 6. Measurement of the MV sensor transfer function.

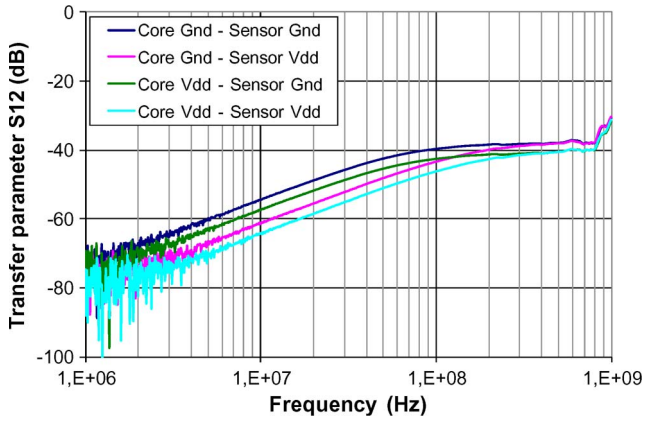

Fig. 7. Measurement of the isolation between the sensor and a digital core.

due to intrinsic noise, interference coupling, and accuracy of equipment used to produce the reference voltage and measure the sensor output. The accuracy of external equipment is given as ± 3 mV. In order to evaluate the measurement accuracy, the repeatability done with each sensor version is measured. For different input voltage values included in the sensor input voltage range, the output signal is sampled ten times at various moments, and the standard deviation of the output sample distribution is computed.

The measurement repeatability is estimated to be ± 4 mV for LV and MV sensors and ± 10 mV for the HV sensor. If the accuracy of external equipment is taken into account, the accuracy of sensor measurements is evaluated to 7 mV for LV and MV sensor versions and 12 mV for the HV sensor version.

3) Transfer Function Characterization: The bandwidth of the sensor is the frequency range over which the pdf of the input signal can be correctly extracted. The sensor bandwidth is limited by the cutoff frequency of the equivalent RC filter composed by the attenuator and the S/H cell. The S/H cell transfer function has been measured by sampling a sinusoidal signal of known amplitude with a varying frequency. The signal is sampled randomly, and the amplitude of the signal is deduced from its pdf. Fig. 6 shows the transfer function measurement of the MV sensor. MV sensors, as LV and HV sensors, exhibit a 3-dB cutoff frequency at 2.5 GHz. The gain of the sensor is nearly constant up to 2.5 GHz. The variation of the gain can be compensated by postprocessing from the transfer function characterization.

4) Effect of Temperature: To ensure the accuracy of measured sampled data, the effect of environmental conditions such as ambient temperature is also evaluated. The I/O characteristic and the transfer functions have been measured at different temperatures, ranging from -40 °C up to 150 °C, controlled by a climatic chamber.

The gain and offset of the sensor are slightly changed. The gain of each sensor tends to decrease linearly with temperature increase (a decrease of 1% for the LV and MV sensors and 6% for the HV sensor). The offset slightly increases with temperature (less than 0.4 mV/°C). Moreover, the amplifier cutoff frequency tends to decrease with temperature (10 kHz/°C). At 150 °C, the cutoff frequency is equal to 600 kHz. When measurements are conducted in a harsh environment, if a very high accuracy is required, sensor performance has to be evaluated to apply data postprocessing in order to compensate gain and offset drifts due to very high or very low temperature.

5) Effect of Electrical Overstress and Aging: During susceptibility tests, the sensor can be exposed to large voltage fluctuations which can accelerate its aging and modify its performances. The sensor's robustness is evaluated by applying an electrical overstress on the sensor input and measuring both the I/O characteristic and the transfer function regularly. The applied stress is a sinusoidal signal centered around the maximum input voltage (3.75, 7.5, and 40 V for the LV, MV, and HV sensors, respectively) with an amplitude that is equal to 20% of the maximum input voltage. After 120 min of electrical stress, the characteristics of the sensor are not affected. The gain has not changed (only -0.7%, -0.2%, and -0.9% for the LV, MV, and HV sensors, respectively), and the variation of the offset is negligible ($+20$, -30, and $+20$ mV for the LV, MV, and HV sensors, respectively).

6) Sensor Isolation Characterization: Voltage fluctuations induced by EMI coupling on the circuit under test can couple to the sensor through its power supply and its substrate. S parameter measurements are performed to characterize the isolation of the sensor from the noise coupled on a given block. Test ports are placed on the power supply and ground pins of a digital core and the sensor that aims at measuring the voltage fluctuations coupled on this digital core. Fig. 7 shows the transfer parameters S12 measured between the different pins, which are less than -30 dB up to 1 GHz.

D. Signal Sampling With the Sensor

The acquired samples form a set of measurements of a random variable. Determining the probability distribution of the measured signal and extracting its statistical characteristics, such as mean, peak-to-peak amplitude, standard deviation, etc., provide valuable information. A histogram is an adapted graphical representation of a probability distribution.

However, it provides only an estimation of the actual probability distribution of the measured signal. The accuracy depends on both the number of samples and the number of bins (i.e., a discrete interval of the measured signal range) which has to be carefully chosen. A small number of bins reduces the resolution of the histogram and degrades the accuracy of the

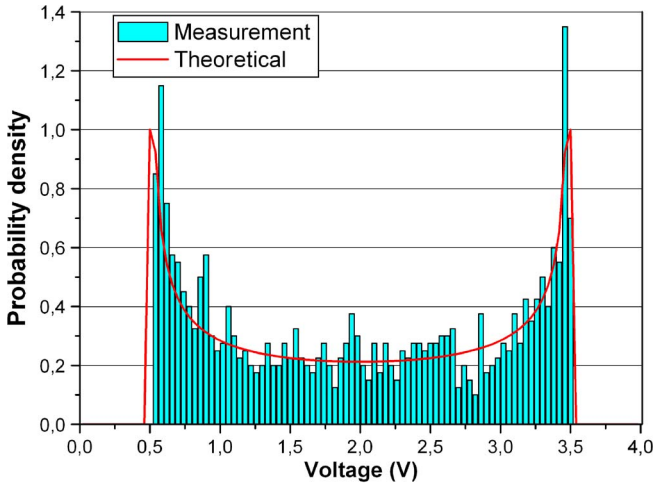

Fig. 8. Measured and theoretical pdfs of a sinusoidal signal.

extraction of statistical properties, while a too large number of bins increases the number of spikes on the histogram. Several theoretical works have attempted to provide algorithms [20] or formulas to find an optimal number of bins N from the number of samples n, such as Sicard–Max or Sturge formula [21]

$$N = 1 + \log_2(n) = 1 + 3.3.\log_{10}(n). \tag{3}$$

A usual choice of bin number is given by the square root choice given by

$$N = \sqrt{n}. \tag{4}$$

However, all of these formulas suffer from the assumption made on the type of distribution and the large number of samples. Therefore, the number of bins can be experimentally set to optimize the number of samples and the histogram resolution. A rule of thumb is to ensure that the bin width remains larger than the measurement resolution. Experimental results have shown that the sensor resolution is about 10 mV.

In order to verify the correctness of probability distribution extracted from sensor measurement, the pdf of a basic signal is measured with the on-chip sensor. Fig. 8 shows the histogram obtained with a sinusoidal signal. The signal frequency is set to 10 MHz, and its peak-to-peak amplitude is equal to 3 V. The signal is randomly sampled 2000 times at 50 kHz. The number of bins is set to 100, and the bin width is equal to 37.5 mV. As shown in Fig. 8, the sensor measurement result is in accordance with the theoretical pdf given by

$$p(x) = \frac{1}{\pi\sqrt{1-x^2}}, \qquad |x| < 1. \tag{5}$$

V. Study of Digital Core Susceptibility With the On-Chip Noise Sensor

The on-chip noise sensor is now used to study the susceptibility of a digital core to conducted interferences coupled on its power supply. Sensor measurements aim at determining the amount of voltage fluctuations induced on the core power supply internally, characterizing the actual susceptibility level of the digital core and understanding the failure mechanism.

A. Case Study and Experimental Setup Description

An LV-range on-chip noise sensor (0–3.75 V) has been placed along the power supply rail of a digital core, in order to measure the amplitude and the statistical distribution of EMI-induced voltage fluctuations. The digital core is composed of a string of buffers which delays an input signal and is terminated by an edge-triggered D flip-flop synchronized by a clock signal. The core is supplied by a dedicated and decoupled 2.5-V power supply. Core I/Os are made of two parts: a level shifter powered by the 2.5-V core power supply and the I/O buffer powered by a dedicated 5-V power supply.

Harmonic disturbances are injected on the digital core power supply pin according to the DPI standard over the range of 1–1000 MHz. The experimental test bench is described in Fig. 9.

The circuit, mounted in a 128 TQFP package, is soldered on a four-layer EMC test board. The 2.5- and 5-V power planes are carefully decoupled and isolated from DPI injection points by choke inductances. During the susceptibility tests, two types of experiments are performed. First, the EMI-induced noise on the core power supply is measured for a constant level of conducted disturbance. The EMI-coupling transfer function, i.e., the ratio between the amplitude of voltage fluctuations and the forward power of the conducted disturbance, can be extracted. In order to demonstrate the relevance of on-chip noise measurements, the EMI-transfer function is extracted by the following.

1) Off-chip measurement: The EMI-induced noise is measured across the core power supply package pin by a 2-GHz digital oscilloscope equipped with a 2.5-GHz active probe.
2) On-chip measurement: The EMI-induced noise is measured internally along the core power supply rail pin by the on-chip noise sensor.

The second experiment consists in correlating core failures induced by conducted interferences with the voltage fluctuations measured by the on-chip noise sensor. Core failures are associated to binary errors and are detected by monitoring the core output signal in the time domain. Two failure criteria are defined to detect core failures.

1) A degradation of the logic level amplitude due to noise coupling. As the required power to induce a change of the logic state of the output signal is very large, we set the maximum allowed noise amplitude to 10% of the nominal power supply (i.e., 0.5 V).
2) A shift of one-half of the clock period (i.e., $\pm$50 ns) of the arrival time of output logic state due to EMI-induced jitter.

B. Off-Chip and On-Chip EMI-Induced Noise Measurements

In order to compare the off-chip and on-chip EMI-coupling transfer functions, the forward power of the conducted interference is measured each time that on-chip and off-chip voltage fluctuations exceed a given voltage value. This voltage value is

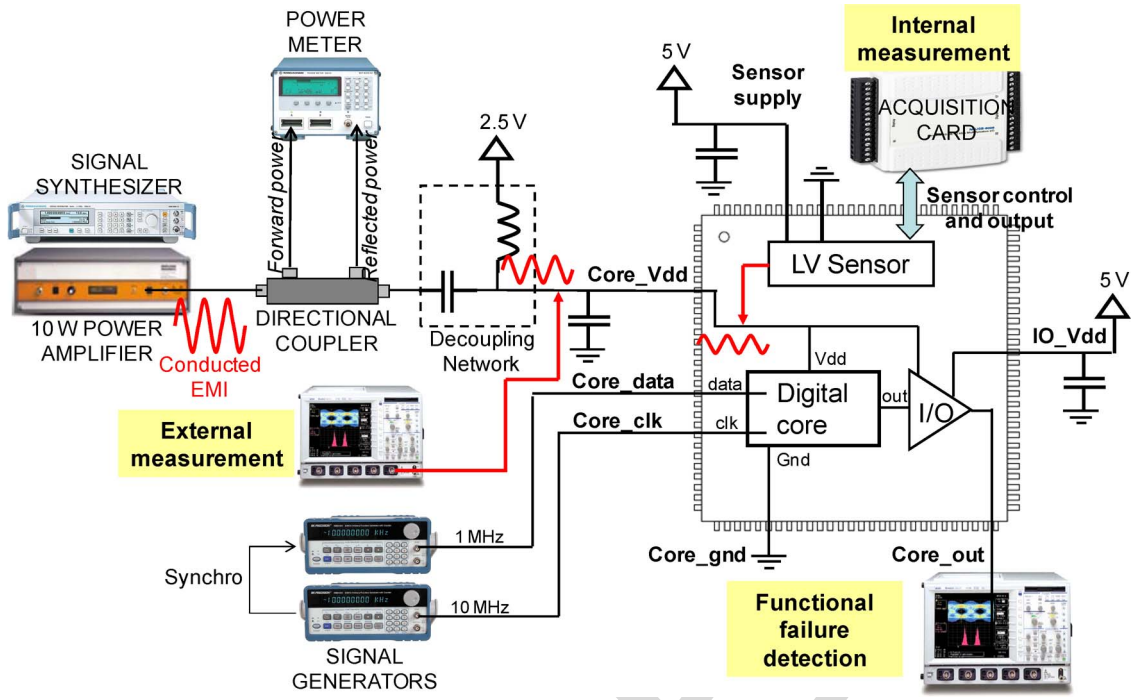

Fig. 9. Experimental setup for the characterization of the conducted susceptibility of the digital core.

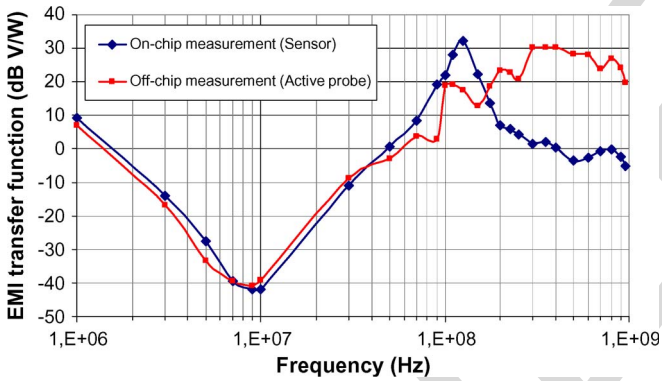

Fig. 10. Comparison of off-chip and on-chip EMI-coupling transfer functions.

set to 0.25 V to ensure a small-signal condition. As harmonic disturbances are injected, this condition can be checked by measuring the symmetry of the pdf of voltage fluctuations.

Fig. 10 shows the comparison of off-chip and on-chip EMI-coupling transfer functions. Below 50 MHz, both measurement methods provide identical results. Off-chip and on-chip voltage fluctuations are identical. Around 10 MHz, the weakness of EMI coupling is explained by the efficiency of the test board decoupling. However, above 50 MHz, both measurement methods give different results. Between 50 and 200 MHz, the on-chip measured EMI-induced noise is larger than that of the off-chip noise. The on-chip EMI coupling is optimized at 140 MHz. Above 140 MHz, the on-chip EMI coupling decreases, and the off-chip noise measurement exceeds the on-chip noise one.

As the cutoff frequencies of both measurement systems exceed 1 GHz, the observed differences cannot be explained by their frequency limits but by the differences in measurement locations. The significant measurement discrepancies between the on-chip and the off-chip EMI-induced noise can lead to different evaluations of circuit susceptibility. These measurements show that the on-chip noise sensor provides a more accurate measurement of EMI coupling across the digital core above 50 MHz. Around 100 MHz, the amount of EMI-induced noise tends to be underestimated by off-chip measurements, while it is overestimated above 200 MHz. Moreover, the complex on-chip propagation of conducted EMI can be understood more clearly by on-chip noise sensor measurements.

C. Analysis of EMI Coupling on Core Power Supply

In order to clarify the origins of differences between off-chip and on-chip measurements, an electrical model of the circuit including the package, the EMC test board, and the DPI test bench has been built. The central part of the model is formed by the PDN of the core. The main elements of the PDN are the physical interconnects of the core power supply rails, the equivalent capacitance of the core, and the I/O pads. An *RC* extraction tool is used to extract the core equivalent capacitance and interconnect resistance. Package pins add parasitic inductances to the core PDN, which can be computed by quasi-static approximations from the package geometrical dimensions.

However, although the power supply domains of the different blocks of the circuit are separated, they can interact due to parasitic couplings. Onboard measurements of EMI propagation between 5- and 2.5-V power planes have shown that parasitic couplings at board level are negligible. At circuit level, two coupling mechanisms predominate. First, as the different blocks of the circuit share the same P^+ substrate, a significant substrate coupling exists between the ground connections of each block. Impedance measurements are performed to extract the resistive network which interconnects the ground connections of the different blocks of the circuit. Second, the core and the I/O

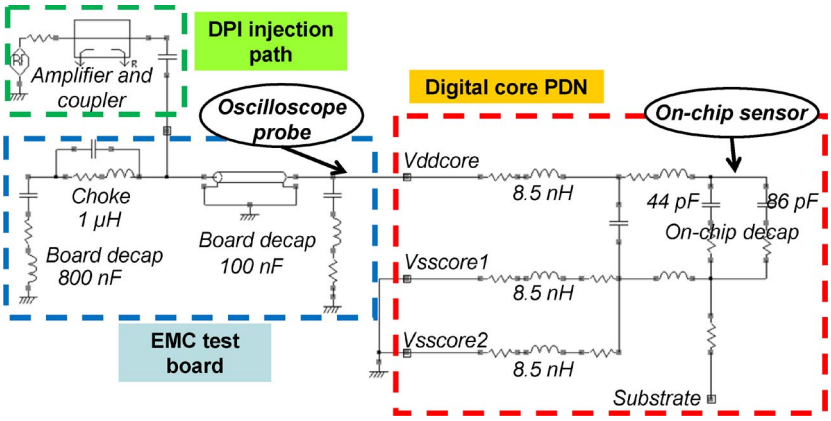

Fig. 11. Model of the digital core PDN including the EMC test board and the DPI injection.

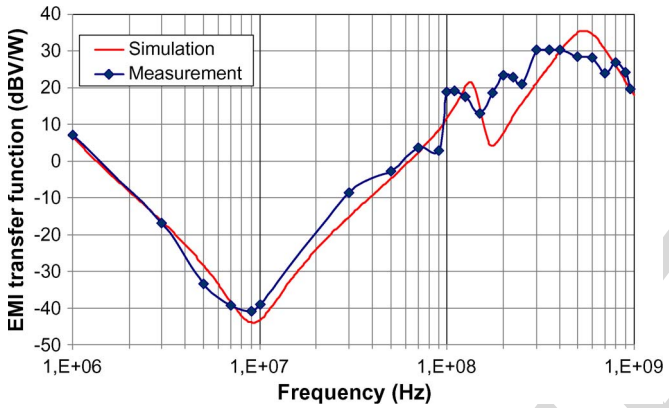

Fig. 12. Comparison between measurement and simulation of off-chip EMI-coupling transfer function.

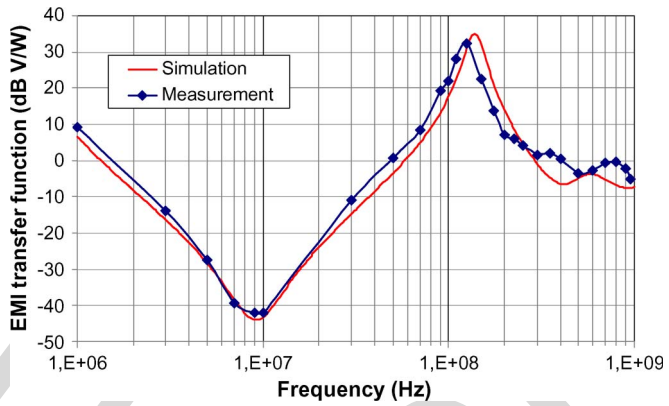

Fig. 13. Comparison between measurement and simulation of on-chip EMI-coupling transfer function.

power supplies are coupled by parasitic capacitors through the ESD protections of core power supply pads. These parasitic capacitors can be estimated by RC extraction.

Finally, S parameter measurements between the different pins of the core PDN are done with high-frequency probes in order to validate the circuit model. A simplified version of the final model is shown in Fig. 11. Positions of voltage probes to extract the off-chip and the on-chip EMI-induced noise are indicated. IC-EMC software [22] is used to perform ac simulations and compute the EMI-coupling transfer functions.

The comparisons between measured and simulated off-chip and on-chip EMI-coupling transfer functions are presented in Figs. 12 and 13, respectively.

The good agreement between simulation and measurement curves validates the circuit model. The slight differences between measurements and simulations are mainly due not only to measurement uncertainties but also to inaccuracies in models of external passive devices, package interconnects, and substrate coupling. The analysis by simulation of the core electrical model helps us to understand the difference between off-chip and on-chip EMI couplings. The circuit package, IC interconnects, and equivalent on-chip capacitance act as a low-pass filter above 50 MHz. The on-chip EMI-coupling optimum measured at 140 MHz is due to the resonance between package inductances and core equivalent capacitance. Above the resonance frequency, the on-chip decoupling filters EMI-induced voltage fluctuations efficiently.

D. Analysis of Core Failure by On-Chip Sensor Measurements

The second part of the experiment aims at correlating the core failures induced by conducted disturbances with sensor measurement to verify the responsibility of the core for failures and determining its sensitivity level to EMI-induced noise. First, the susceptibility level of the core is measured according to the DPI test setup described in Fig. 9. Fig. 14 shows the amount of forward power of the conducted harmonic disturbance to induce a core failure. The power amplifier can deliver up to 40 dBm without saturation. Two types of failures arise: either timing jitter on the core output signal or a degradation of logic levels due to an excessive noise. For each test frequency, the type of failure is pointed out on the curve. Below several megahertz, conducted disturbances lead to a significant timing jitter, while they disturb output signal logic levels above several tens of megahertz.

The susceptibility threshold can be compared to the on-chip EMI transfer function (Fig. 13). The circuit sensitivity to EMI is very weak between 2 and 50 MHz because the coupling of EMI is not efficient over this frequency range due to board decoupling. As the EMI coupling on the core power supply node is the most efficient at 140 MHz, we can expect a marked sensitivity of the circuit around this frequency. Although a susceptibility peak appears at 140 MHz, the circuit is the more sensitive at 500 and 950 MHz. Above 200 MHz, the

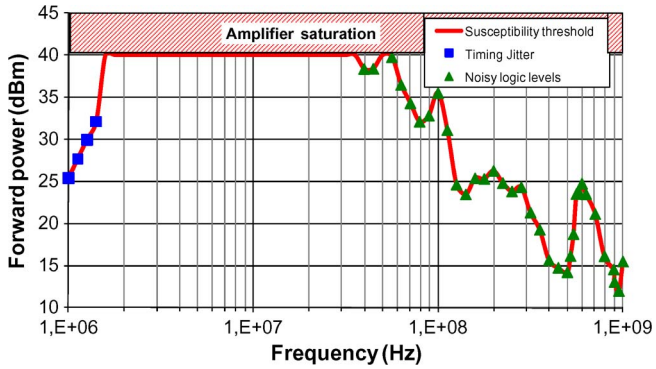

Fig. 14. Measurement of the susceptibility threshold of the digital core.

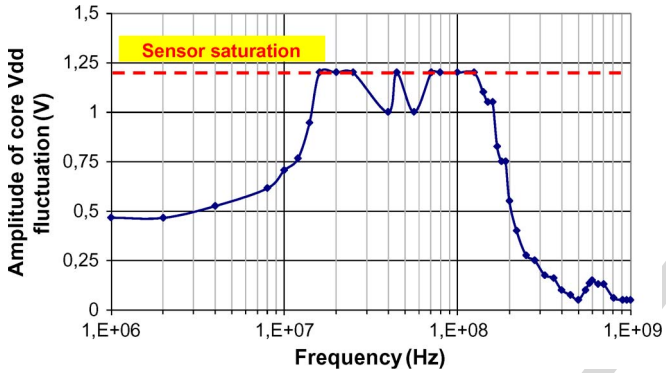

Fig. 15. Measurement of the amplitude of digital core power supply voltage fluctuation at failure occurrence.

susceptibility of the core no longer seems correlated to power supply voltage fluctuations.

The on-chip noise sensor is used to correlate failure occurrences and the amount of noise induced on core power supply. At each disturbance frequency, the amplitude of the core power supply voltage fluctuation is picked up when a failure arises or when the power amplifier saturates, and is reported on the graph in Fig. 15. As the nominal core power supply is equal to 2.5 V and the LV sensor range is limited to 3.75 V, the sensor output saturates when the voltage fluctuation amplitude exceeds 1.2 V.

On-chip noise sensor measurement shows that the core failures are strongly linked to core power supply voltage fluctuations up to 160 MHz. Below 10 MHz, the circuit is very sensitive to core power supply voltage fluctuations which induce timing jitter on the output signal. The sensitivity level of the core tends to decrease at higher frequency. As explained in [23], the amount of EMI-induced jitter which affects digital gates is not only proportional to the EMI amplitude but also frequency dependent. For a constant level of EMI, the induced jitter tends to reduce when the frequency increases. Between 20 and 160 MHz, failure occurs for a nearly constant level of voltage fluctuation, very close to the saturation level of the sensor. When the core power supply ripple exceeds 1.25 V (half of the core power supply voltage), the core operation is strongly affected, and the output signal logic levels starts to be altered.

However, above 160 MHz, failures happen without significant core power supply voltage fluctuations. The degradation of the output signal can no longer be explained by the disturbance of the core operation, but it seems to be linked to a direct disturbance of the output buffer. The failure mechanism of the digital core to conducted interferences along the core power supply includes not only the core but also the output buffer. This hypothesis about the origin of the failure is studied with an additional on-chip sensor measurement in the following part.

E. Analysis of I/O Failure by On-Chip Sensor Measurements

Although core and I/O supply domains are separated, they are connected by ESD protections and coupled by parasitic capacitances associated to ESD protections and core power supply pads. A sensor placed on the output buffer power supply could confirm the hypothesis of a noise coupling between core and output buffer power supplies, but unfortunately, it has not been planned at test chip specification. However, a similar I/O has been isolated with 2.5- and 5-V power supplies for the level shifter and the output buffer, respectively. An MV-range on-chip sensor has been placed on the output buffer power supply to monitor voltage fluctuations.

This sensor can be used during conducted injection on the 2.5-V power supply of the level shifter to have a qualitative evaluation of the impact of the parasitic coupling between core and output buffer power supplies. This measurement done on the isolated I/O block does not give us directly the exact level of coupling between digital core and output buffer since I/O and digital core blocks have different PDNs. However, we can expect to observe similar effects because the PDN structure is the same for both blocks. The proposed measurement aims at highlighting a possible significant coupling between digital core and output buffer power supplies and detecting a frequency range where the output buffer power supply is disturbed by the conducted injection done on core power supply.

A DPI injection is performed on the level shifter power supply of the isolated I/O. Only failures associated to a degradation of the logic level amplitude of the output signal appear. When a failure arises (if the noise amplitude on the output signal exceeds 0.5 V), the amplitude of the noise induced on the output buffer power supply is measured with the on-chip sensor. The experimental test bench is shown in Fig. 16.

The sensor measurement of the noise coupled on the output buffer power supply is shown in Fig. 17. The voltage fluctuation remains negligible when a failure arises below 100 MHz, so the noise measured on the output signal is not related to the output buffer power supply voltage fluctuation but to that of the level shifter power supply. The comparison with sensor measurement on core power supply shows that the failure is only linked to the core, not to the output buffer. However, the noise coupled on the output buffer power supply becomes very significant between 100 and 450 MHz. Moreover, it becomes large enough to trigger ESD protections between both power supply domains and corrupt the logic level of the output signal. Over this range, the I/O failure is due to the coupling of conducted noise on the output buffer power supply which disturbs the output buffer operation. The increase of the output buffer power supply voltage fluctuation can be compared to the reduction of that of

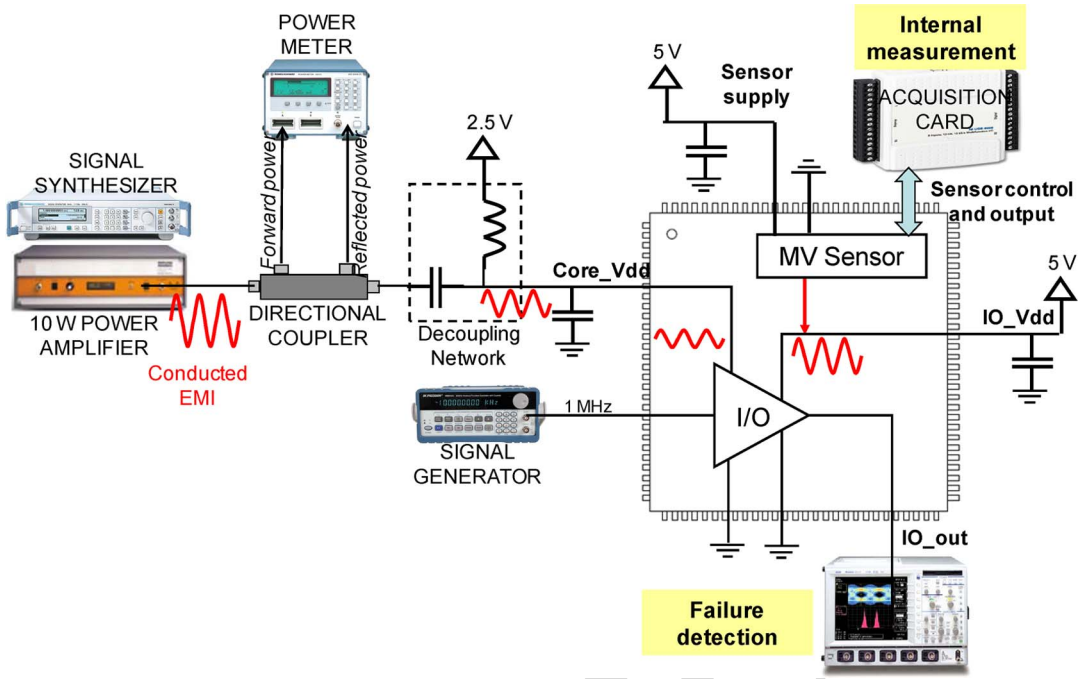

Fig. 16. Experimental setup for the characterization of the coupling between core and I/O power supplies.

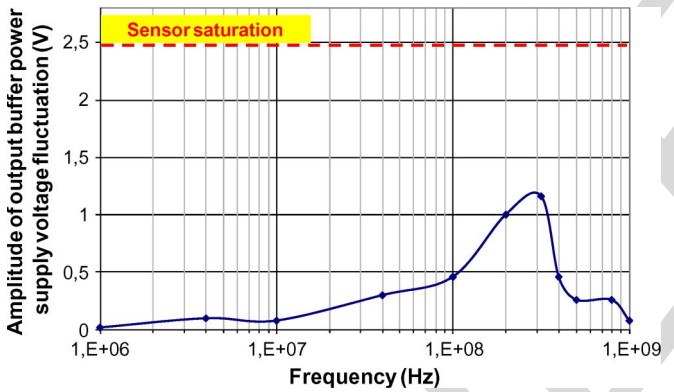

Fig. 17. Measurement of the amplitude of output buffer power supply voltage fluctuation at failure occurrence.

the core power supply over the same frequency range (Fig. 15). The combination of on-chip noise measurement on core and output buffer power supplies confirms that the output buffer has a significant impact on the digital core failure mechanism.

Above 450 MHz, the noise amplitude on the output buffer power supply is reduced. The I/O failure seems to be no longer associated to output buffer power supply fluctuations. The on-chip sensor measurements on core and output buffer power supplies fail to provide a satisfactory explanation of the digital core failure mechanism above 450 MHz. The coupling of EMI on other nodes of the circuit is responsible of the observed failures. For example, the output node of the core is strongly affected by EMI-induced noise, externally coupled through the PCB. Experimental observations show that, above a certain amplitude, the noise on the output signal is able to trigger ESD protections. A more accurate understanding of the core failure could be obtained by placing a larger number of sensors over the digital core, particularly on the core output node.

VI. Conclusion

This paper has presented an on-chip sensor dedicated to the characterization of circuit susceptibility, based on a random subsampling of voltage fluctuations across sensitive nodes. Although this acquisition mode does not allow a reconstruction of signal waveform in time domain, the amplitude of EMI-induced voltage fluctuations and signal distortions can be extracted without complex experimental setup and postprocessing. Several versions of this sensor have been developed in 0.25-μm CMOS process for various voltage ranges. The main advantages of this sensor are its small surface, its large bandwidth (up to 2 GHz in the LV range), its high linearity, and robustness to electrical stress, at the price of a simple design.

This sensor has been used to study the susceptibility of a digital core to conducted disturbances. On-chip sensor measurements offer a more accurate evaluation of EMI-induced noise than off-chip measurements above several tens of megahertz because of the package and circuit filtering effect. For circuit designers, using this type of on-chip sensor is of great interest because it provides a precise characterization of noise propagation within the die and helps to identify the sensitive blocks, extract their actual susceptibility level, and validate their models. Placing a network of such a sensor on each sensitive node of a circuit (e.g., power supply and ground rails, sensitive input, reference voltage, etc.) could facilitate failure diagnosis and the modeling of complex parasitic couplings between separated blocks, such as substrate coupling, crosstalk, etc.

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On-Chip Noise Sensor for Integrated Circuit Susceptibility Investigations

Sonia Ben Dhia, *Member, IEEE*, Alexandre Boyer, Bertrand Vrignon, Mikaël Deobarro, and Thanh Vinh Dinh

***Abstract*—With the growing concerns about electromagnetic compatibility of integrated circuits, the need for accurate prediction tools and models to reduce risks of noncompliance becomes critical for circuit designers. However, an on-chip characterization of noise is still necessary for model validation and design optimization. Although different on-chip measurement solutions have been proposed for emission issue characterization, no on-chip measurement methods have been proposed to address the susceptibility issues. This paper presents an on-chip noise sensor dedicated to the study of circuit susceptibility to electromagnetic interferences. A demonstration of the sensor measurement performances and benefits is proposed through a study of the susceptibility of a digital core to conducted interferences. Sensor measurements ensure a better characterization of actual coupling of interferences within the circuit and a diagnosis of failure origins.**

***Index Terms*—Electromagnetic compatibility (EMC), integrated circuits (ICs), interference measurement, on-chip sensor, susceptibility testing.**

I. Introduction

THESE LAST years, the concerns about electromagnetic compatibility (EMC) of integrated circuits (IC; emission and susceptibility issues) have grown considerably. The need for prediction of noncompliance risks during the design stage has become critical for IC manufacturers in order to reduce redesign costs and time to market [1]. Although several tools and prediction methodologies have been developed recently [2], [3], accurate measurements of on-chip noise are still critical information for designers for model validation and design optimization.

The external characterization of fast transient current induced by circuit activity is limited by the bandwidth of CMOS analog buffer and electrical parasitic elements of chip and package interconnects. Numerous on-chip measurement devices have been proposed over the last 15 years, and published results have demonstrated the positive contribution of on-chip measurements to characterize accurately and solve power integrity, simultaneous switching noise, ground bounce, crosstalk, or substrate coupling issues. The different systems for on-chip noise characterization can be classified into two families: the on-chip waveform capturing circuits and the noise detectors. Most on-chip waveform capturing circuits are based on a subsampling cell [4], [5] dedicated to repetitive signal measurements with very small time resolution, comprised between 100 ps [6] and 10 ps [7], [8]. Despite excellent time resolution characteristics, the circuit under test must operate in a special mode where a periodic event is generated, so the noise produced during normal operating mode cannot be characterized. In [9], the use of two subsampling cells allows the extraction of the signal autocorrelation and, thus, its power spectral density without requiring repetitive chip operations. Noise waveforms can also be measured by built-in probing techniques which rely on small voltage-to-current converter cells [10] and can be distributed over IC power distribution networks (PDNs) to obtain a noise distribution map [11]. The second category, i.e., the noise detectors, aims at providing the primary characteristics of noise without acquiring the timing waveform. Their advantage lies in the reduced amount of data to process to obtain information about on-chip noise. In [12], an on-die droop detector is presented. Amplitude, duration, and polarity of power supply fluctuations are characterized in real time by comparing signals to programmable thresholds. Only significant events are characterized by the noise detector which transmits 1 b per acquisition.

However, although on-chip noise measurement techniques have been used for power integrity and conducted emission characterization in digital ICs, they have never been used for the characterization of susceptibility to electromagnetic interferences (EMIs). Susceptibility of ICs has become one of the major issues for all circuit classes (digital, analog, RF, and power). Concerns about failure mechanisms, EMI coupling, and susceptibility modeling at circuit level have arisen recently [13]. The main problem for IC designers is to be able to evaluate the compliance according to standard susceptibility tests prior to circuit fabrication. The susceptibility of a circuit depends not only on the intrinsic sensitivity of disturbed functions to EMI-induced voltage fluctuations but also on the filtering effect of package bonding wires, chip interconnects, on-chip decoupling, substrate coupling, etc.

In this context, measuring the amount of EMI-induced noise on a sensitive node of a circuit is critical for IC designers for two reasons. First, an accurate measurement of parasitic voltage fluctuations on circuit terminals helps to determine the actual

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sensitivity of the disturbed function. Thus, if this measurement confirms that a susceptibility peak is linked to an efficient coupling of the EMI within the circuit, designers should try to enhance the filtering effect of the circuit at this particular frequency (e.g., by adjusting on-chip decoupling capacitance value). Second, comparing measurements to simulation results can help to validate circuit susceptibility models.

This paper aims at presenting an on-chip sensor dedicated to the characterization of the EMI-induced noise during standard immunity tests and demonstrating through a case study how it can be helpful in solving susceptibility issues. Section II presents briefly a state of the art of standard methods for IC susceptibility characterization. Their limitations in precisely extracting the actual susceptibility level of a circuit compared to an on-chip measurement are explained, and the general requirements of an on-chip noise sensor for IC susceptibility characterization are introduced. In Section III, the acquisition technique and the sensor architecture are presented. Section IV describes the sensor design and the experimental characterization of sensor performances. In Section V, the sensor is used to study the susceptibility of a digital core to conducted EMI experimentally.

II. Measurement of EMI-Induced Noise for IC Susceptibility Characterization

A. IC Susceptibility Characterization

Susceptibility tests aim at characterizing sensitivity level of electronic equipment to conducted or radiated EMIs and ensuring the compliance to limits defined by standards or customer requirements. Susceptibility test setup definitions and recommendations are given by standards such as CISPR 25 [14]. The susceptibility of equipment depends not only on numerous parameters, e.g., shielding effectiveness, printed circuit board (PCB) routing, decoupling, filtering, etc., but also on circuit susceptibility. Thus, EMC requirements at equipment level are laid down for ICs. IC manufacturers are forced to qualify the susceptibility of their devices and ensure the compliance with customer requirements.

Specific standards have been defined to test the susceptibility of IC, such as IEC 62132 [15]. This standard widely used by IC manufacturers proposes different types of tests to characterize IC sensitivity to conducted or radiated EMI up to 1 GHz. For diagnosis purposes and precompliance tests, IC manufacturers usually use the IEC 62132-4—direct power injection (DPI) method [16], based on conducted EMI injections applied on one or several pins.

B. Limitation of External Characterization of IC Susceptibility

Immunity test methods defined by IEC 62132 give indications about the IC behavior exposed to RF disturbances by an external observation of voltage or current waveforms. The propagation of the RF interference through package and circuit interconnects, its penetration efficiency, and the coupling path dependence on frequency remain unknown. Moreover, the actual immunity level of the circuit, i.e., the required voltage fluctuation magnitude applied across circuit terminals to induce a failure, is not evaluated.

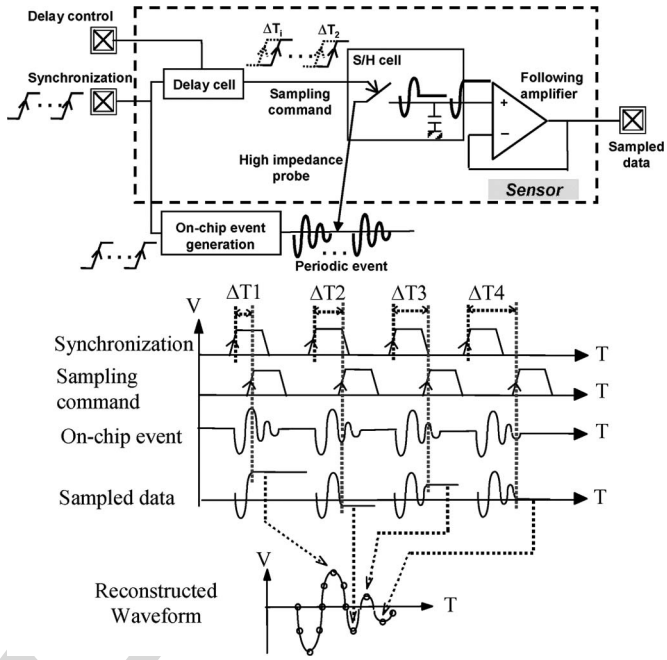

Fig. 1. Original synchronous on-chip noise sensor architecture and sequential equivalent-time sampling principle [17].

Due to the filtering effect of package, circuit interconnects, and bandwidth limitation of output buffers, off-chip measurement fails to provide accurate characterization of EMI-induced noise within circuits over several tens of megahertz. The accurate characterization of the actual susceptibility level of a circuit relies on a low intrusive and wideband on-chip measurement of EMI-induced voltage, i.e., at least the frequency range specified by IEC 62132 (150 kHz–1 GHz). The sensor must measure the voltage amplitude of EMI-induced noise across all types of nodes and withstand electrical overstress without large variations of its performances. Parasitic couplings with other blocks of the circuit must be reduced to prevent from disturbances of measurement. Moreover, the sensor must occupy a small area and a reduced I/O number to simplify its insertion in an existing design.

III. On-chip Noise Sensor Description

A. Synchronous On-Chip Noise Sensor

A first version of the on-chip noise sensor was designed in the early 2000s to address signal and power integrity issues at circuit level [17], [18]. The sensor is based on a sequential equivalent-time sampling [19]. Its architecture and the principle of signal reconstruction are described in Fig. 1.

An on-chip sample and hold (S/H) circuit directly probes the voltage along the circuit interconnects and operates in subsampling conditions. The probe input impedance is large enough to ensure a noninvasive measurement. The signal acquisition is made over several occurrences of a reproducible phenomenon, and only one sample is taken at each repetition. An external synchronization signal is used to trigger off the on-chip event

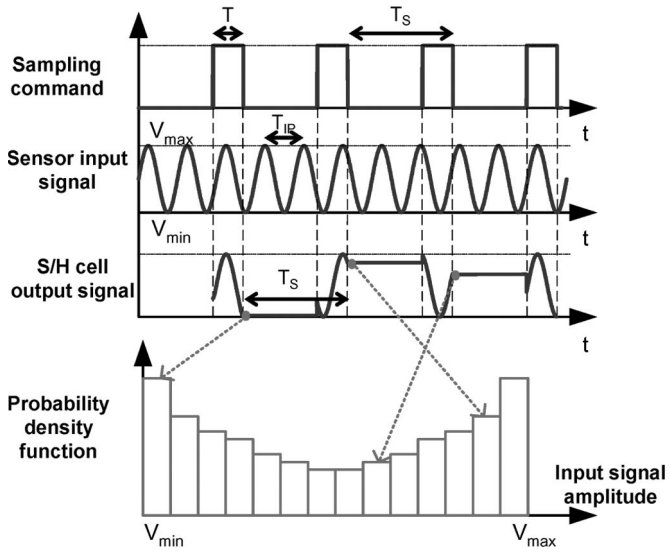

Fig. 2. Asynchronous sampling of a signal and extraction of pdf of the signal amplitude.

to both characterize and activate the S/H cell. The sampling command is shifted from the synchronization signal by a delay cell. The time resolution of the reconstructed waveform is set by the minimum delay step, while its duration is set by the maximum delay produced by the delay cell. Samples are externally stored for waveform reconstruction. A very high virtual sample rate can be reached without severe constraints on hardware bandwidth.

B. Asynchronous On-Chip Noise Sensor

The reconstruction of EMI-induced noise waveform based on sequential equivalent time is difficult. By definition, the EMI characteristics are unknown (amplitude, frequency, and waveform). Waveform reconstruction of the EMI-induced noise relies on acquisitions triggered on a repeatable external interference, which is possible only if the characteristics of the interference are known in advance. However, this condition is usually not ensured, so the signal is sampled at random instants and the waveform cannot be reconstructed.

Nevertheless, even if the sampling cannot be synchronized with the interference, an asynchronous or random sampling can provide valuable information about EMI-induced noise properties. The proposed sensor reuses the same architecture but operates in an asynchronous sampling mode. The S/H cell and the output amplifier are kept, but the delay cell is removed. A low-frequency trigger commands the S/H cell to randomly subsample the input signal. The value stored at the S/H cell output is a random variable which constitutes the outcome of the instantaneous amplitude of input signal measurement. As explained in Fig. 2, this random acquisition allows the extraction of signal amplitude probability density function (pdf) [20]. The pdf provides the likelihood of the input signal having a given amplitude at any time. Whatever the input signal frequency, the pdf of the signal amplitude can be correctly extracted provided that the S/H cell or the output amplifier does not distort or filter the sampled signal.

This acquisition mode can provide valuable information about circuit susceptibility. First, for a given type of disturbance, the average amplitude of the EMI-induced noise can be extracted from the signal amplitude pdf. Moreover, for large-amplitude-disturbance injection, changes in amplitude pdf shape suggest that some distortions induced by the circuit (e.g., electrostatic discharge (ESD) clamp devices triggered by large disturbances) affect the signal.

IV. Sensor Design and Characterization

A. Test Chip Description

The asynchronous on-chip noise sensor has been implemented in a 0.25-μm SMARTMOS 8 technology test chip from Freescale Semiconductor. This technology aims at designing digital and high-voltage (HV) analog mixed circuit that can withstand voltages up to 80 V. The test chip is dedicated to the susceptibility characterization of various analog and digital structures. Ten on-chip sensors have been implemented to monitor power supply voltage fluctuation as close as possible to each block. Moreover, three different sensors have been duplicated for calibration purpose.

B. Design of the On-Chip Noise Sensor

General Architecture: Fig. 3 shows the architecture of the on-chip noise sensor. The sensor is made of three main elements: an attenuator, an S/H cell which operates in subsampling mode, and an output amplifier. The attenuator and the S/H cell form a high-impedance probe which ensures a low intrusive voltage measurement. Three sensor versions have been designed to measure voltage fluctuation in the different power supply domains of the circuit (2.5, 5, and 12 V): low-voltage (LV) range (0–3.75 V), medium-voltage (MV) range (0–7.5 V), and HV range (0–40 V) versions. They are based on the same architecture and use the same S/H cell and operational amplifier. They only differ from the attenuator ratio of the input attenuator. Table I gives the characteristics in terms of voltage range and the gain of the different parts of the three sensor versions.

The sensor response is sensitive to voltage fluctuations coupled on its power supply and its substrate reference. The isolation of the sensor to external disturbances and to noise produced by the other blocks of the circuit is a critical requirement. Thus, the output amplifier and sensor input–output (I/O) are supplied by an external and dedicated 5-V power supply. At board level, this power supply is separated and carefully decoupled. The S/H cell and the amplifier input stage are supplied by a quiet 2.5-V power supply provided by an internal built-in voltage regulator and powered by the 5-V sensor power supply. To prevent from interference coupling on the sensor by the substrate, all the devices of the sensor are isolated from the P substrate by a buried n-layer and dielectric-filled trenches on the sides.

Attenuator Design: The attenuator and the S/H cell are the most critical parts of the sensor to ensure a large bandwidth, improve the linearity, and reduce the voltage dependence. They

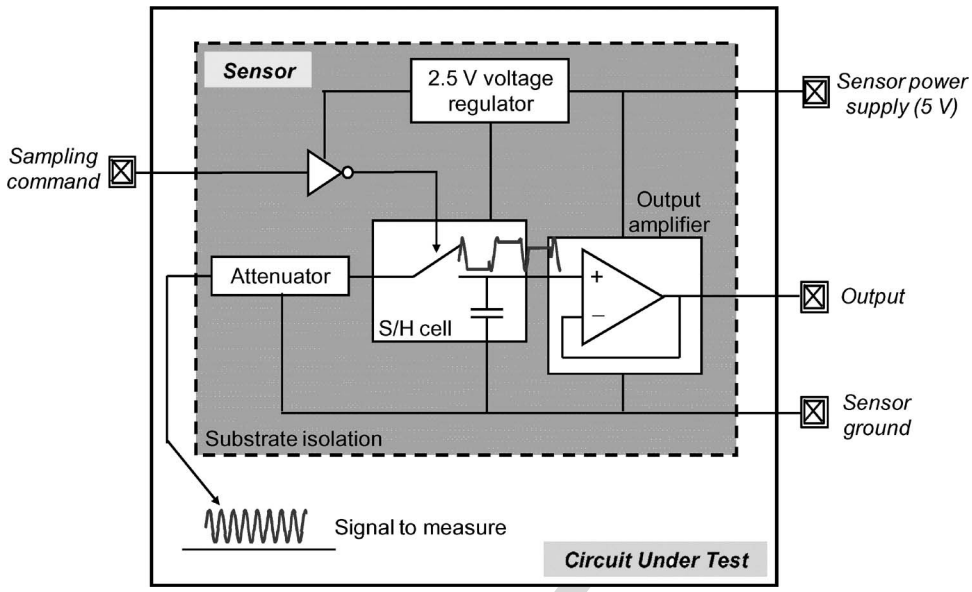

Fig. 3. Asynchronous on-chip noise sensor architecture.

TABLE I
CHARACTERISTICS OF THE THREE SENSOR VERSIONS

Sensor version	Input signal range	Attenuator ratio	Amplifier gain	Output range
Low voltage	0 to 3.75 V	2/3	2	0 to 5 V
Medium voltage	0 to 7.5 V	1/3	2	0 to 5 V
High voltage	0 to 40 V	1/16	2	0 to 5 V

are made of isolated LV transistors to prevent the impact of external disturbance and reach a 2-GHz bandwidth. Fig. 4 shows the electrical schematic of the attenuator and the S/H cell with parasitic elements.

The attenuator is based on a resistive voltage divider made of polysilicon resistor. Polysilicon resistors are designed above thick oxide to withstand voltage up to 80 V. Polysilicon capacitors C_1 and C_2 are added to compensate the parasitic capacitance of the resistors (C_{R1} and C_{R2}) and maintain a flat frequency response. The expression of the transfer function $K(\omega)$ of the attenuator is given by

$$K(\omega) = \frac{R_2}{R_1 + R_2} \frac{1 + jR_1(C_1 + C_{R1})\omega}{1 + j\frac{R_1 R_2}{R_1 + R_2}(C_1 + C_{R1} + C_2 + C_{R2})\omega} \quad (1)$$

The compensation capacitance values are chosen according to

$$C_1 + C_{R1} = \frac{R_2}{R_1}(C_2 + C_{R2}). \quad (2)$$

in order to make the pole and the zero of $K(\omega)$ equal.

The values of resistors, and parasitic and compensation capacitors of the attenuators are reported in Table II. The input impedance of the attenuator is larger than 500 Ω up to 2 GHz for the three sensor versions, which is large enough to ensure a noninvasive voltage measurement.

S/H Cell Design: The S/H cell is composed of a transmission gate switch and a storage node composed of parasitic capacitors of the switch, input capacitor of the amplifier, and the storage capacitor. The sizes of the transmission gate transistors are carefully chosen to optimize the bandwidth and reduce the voltage dependence of the ON-state resistance. However, when the S/H cell turns off, a charge injection in the parasitic capacitances between the control signal and the storage node arises. A parasitic offset can be induced on the output voltage. Despite a reduction of the bandwidth, this effect can be reduced by increasing the storage capacitor. Moreover, adding a dummy transmission gate can help to compensate the charge injection effect.

Output Amplifier Design: An analog output signal is driven off the chip, externally stored, and processed by a digital acquisition card. An on-chip analog-to-digital converter could prevent noise coupling on the sensor output signal, but it also increases the sensor size and the number of I/Os. This integration gain comes with special cares in terms of cable shielding, grounding, and output signal processing. As the S/H cell output signal is constant, the noise can be filtered by averaging several samples. Moreover, as sensor I/O shares the same power supply than output amplifier, the sampling command can induce switching noise along this power supply. The sampling of the sensor output signal has to be done far from sampling command transitions.

The output amplifier is a noninverting CMOS amplifier with a gain of two, made of a 2.5-V rail-to-rail input stage and a 5-V AB class output stage. The output stage has been optimized to keep a constant gain of up to 2.5 MHz and reduce parasitic offset and stability issues. The bandwidth of the output amplifier does not affect the sensor bandwidth since the amplifier does not process the sensor input signal, but the S/H output signal. However, the sampling frequency has to be smaller than the amplifier cutoff frequency to prevent the filtering of the sampling signal, which can affect the measured pdf.

On-Chip Sensor Overall Design: The size of the complete sensor in CMOS 0.25 μm is about 200 μm per 300 μm. Table III gives the size of the different sensor parts. A large part of the sensor is occupied by the output amplifier and the voltage

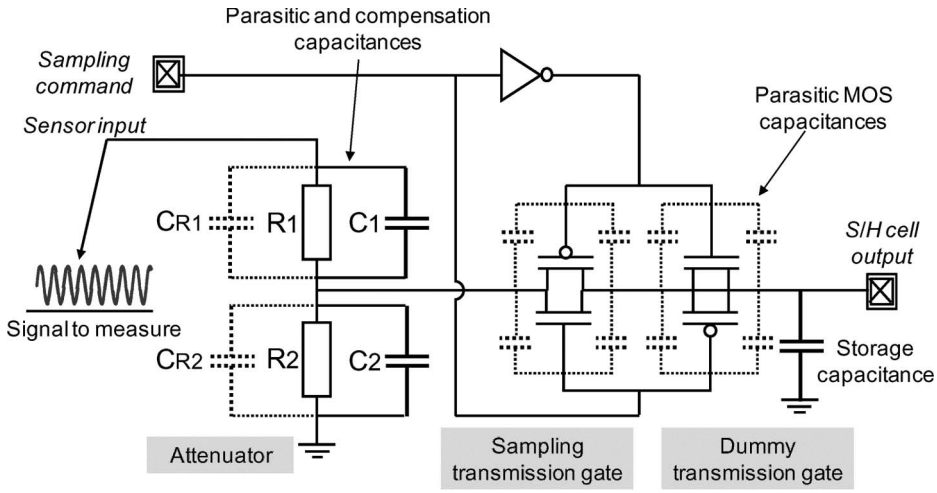

Fig. 4. Schematic of the attenuator and the S/H cell.

TABLE II
CHARACTERISTICS OF ATTENUATOR FOR THE THREE SENSOR VERSIONS

Sensor version	R1 (Ω)	R2 (Ω)	CR1 (F)	CR2 (F)	C1 (F)	C2 (F)
Low voltage	2480	4950	18 f	36 f	400 f	200 f
Medium voltage	9900	4950	71 f	36 f	50 f	200 f
High voltage	38700	2580	16 f	1.1 f	115 f	2 p

TABLE III
CMOS 0.25-μm SENSOR SURFACE

	Width x Length (μm)
Output amplifier	280 x 120
Voltage regulator	270 x 80
Attenuator and S/H cell	20 x 200
Sensor surface	300 x 200

regulator. The total surface of all the sensors of the circuit could be reduced if the output amplifier and the voltage regulator are shared by all the sensors and the outputs of all S/H cells are multiplexed on the common output amplifier.

C. Characterization of the Sensor

In this part, the complete characterization of the sensor performances (I/O characteristic, transfer function, sensitivity to temperature, and aging) is presented. The characterization of the sensor is necessary to calibrate the sensor, i.e., compensate the nonideal behavior of the sensor.

1) Sensor Calibration Procedure: The sensor operation is affected by imperfections and mismatch in the implementation of its elements, which degrades the output responses. The output amplifier is not perfectly linear, so the gain is not constant. Moreover, errors in attenuator resistance values can change the gain of the sensor. Moreover, both the amplifier and the parasitic capacitance of the S/H cell produce an offset voltage. The I/O characteristic is measured to check the sensor linearity and then calibrate the sensor. It consists in applying a constant and known voltage on the sensor input and measuring the voltage amplitude of the output samples. A linear relation

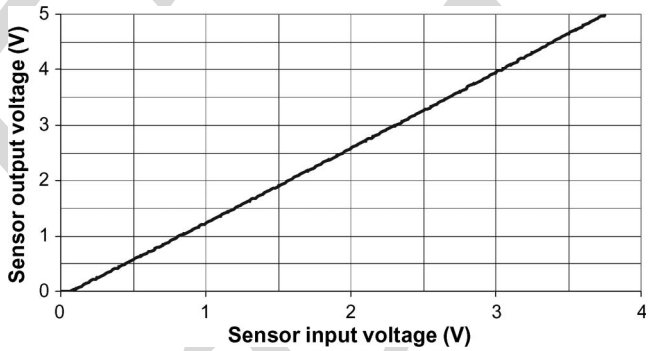

Fig. 5. LV sensor I/O characteristic.

TABLE IV
SENSOR GAIN AND OFFSET CHARACTERIZATION

Sensor version	Theoretical gain	Measured gain	Measured offset
Low voltage	1.333	1.353	100 mV
Medium voltage	0.667	0.677	1 mV
High voltage	0.125	0.134	3 mV

can be established between sensor output and input. From this relation, both static gain and offset can be extracted to compensate sensor imperfections. The LV sensor is highly linear above 0.15 V, as shown in Fig. 5. The MV and HV sensors are also linear above 0.3 V and between 3 and 37 V, respectively. The measured gain and offset for the three sensor versions are reported in Table IV.

2) Accuracy of Sensor Measurements: The I/O characteristic shown in Fig. 5 makes the link between the actual and the measured voltage levels and compensates the systematic errors due to sensor imperfections. However, this characterization and the measurement repeatability are disturbed by random errors

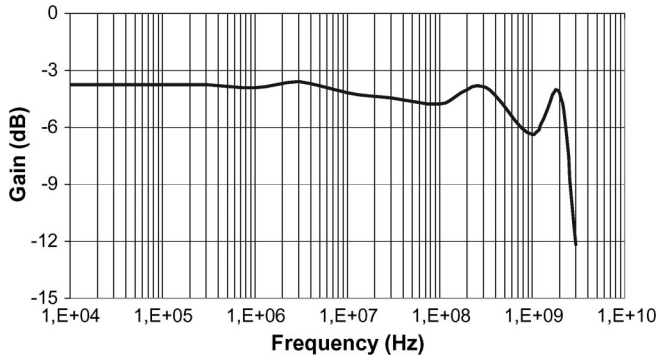

Fig. 6. Measurement of the MV sensor transfer function.

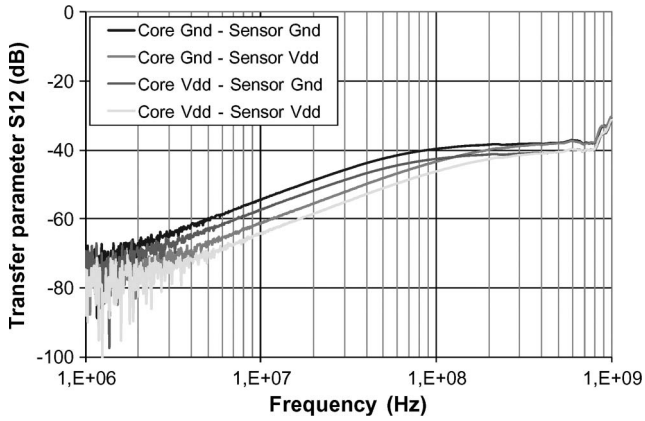

Fig. 7. Measurement of the isolation between the sensor and a digital core.

due to intrinsic noise, interference coupling, and accuracy of equipment used to produce the reference voltage and measure the sensor output. The accuracy of external equipment is given as ± 3 mV. In order to evaluate the measurement accuracy, the repeatability done with each sensor version is measured. For different input voltage values included in the sensor input voltage range, the output signal is sampled ten times at various moments, and the standard deviation of the output sample distribution is computed.

The measurement repeatability is estimated to be ± 4 mV for LV and MV sensors and ± 10 mV for the HV sensor. If the accuracy of external equipment is taken into account, the accuracy of sensor measurements is evaluated to 7 mV for LV and MV sensor versions and 12 mV for the HV sensor version.

3) Transfer Function Characterization: The bandwidth of the sensor is the frequency range over which the pdf of the input signal can be correctly extracted. The sensor bandwidth is limited by the cutoff frequency of the equivalent RC filter composed by the attenuator and the S/H cell. The S/H cell transfer function has been measured by sampling a sinusoidal signal of known amplitude with a varying frequency. The signal is sampled randomly, and the amplitude of the signal is deduced from its pdf. Fig. 6 shows the transfer function measurement of the MV sensor. MV sensors, as LV and HV sensors, exhibit a 3-dB cutoff frequency at 2.5 GHz. The gain of the sensor is nearly constant up to 2.5 GHz. The variation of the gain can be compensated by postprocessing from the transfer function characterization.

4) Effect of Temperature: To ensure the accuracy of measured sampled data, the effect of environmental conditions such as ambient temperature is also evaluated. The I/O characteristic and the transfer functions have been measured at different temperatures, ranging from -40 °C up to 150 °C, controlled by a climatic chamber.

The gain and offset of the sensor are slightly changed. The gain of each sensor tends to decrease linearly with temperature increase (a decrease of 1% for the LV and MV sensors and 6% for the HV sensor). The offset slightly increases with temperature (less than 0.4 mV/°C). Moreover, the amplifier cutoff frequency tends to decrease with temperature (10 kHz/°C). At 150 °C, the cutoff frequency is equal to 600 kHz. When measurements are conducted in a harsh environment, if a very high accuracy is required, sensor performance has to be evaluated to apply data postprocessing in order to compensate gain and offset drifts due to very high or very low temperature.

5) Effect of Electrical Overstress and Aging: During susceptibility tests, the sensor can be exposed to large voltage fluctuations which can accelerate its aging and modify its performances. The sensor's robustness is evaluated by applying an electrical overstress on the sensor input and measuring both the I/O characteristic and the transfer function regularly. The applied stress is a sinusoidal signal centered around the maximum input voltage (3.75, 7.5, and 40 V for the LV, MV, and HV sensors, respectively) with an amplitude that is equal to 20% of the maximum input voltage. After 120 min of electrical stress, the characteristics of the sensor are not affected. The gain has not changed (only -0.7%, -0.2%, and -0.9% for the LV, MV, and HV sensors, respectively), and the variation of the offset is negligible ($+20$, -30, and $+20$ mV for the LV, MV, and HV sensors, respectively).

6) Sensor Isolation Characterization: Voltage fluctuations induced by EMI coupling on the circuit under test can couple to the sensor through its power supply and its substrate. S parameter measurements are performed to characterize the isolation of the sensor from the noise coupled on a given block. Test ports are placed on the power supply and ground pins of a digital core and the sensor that aims at measuring the voltage fluctuations coupled on this digital core. Fig. 7 shows the transfer parameters S12 measured between the different pins, which are less than -30 dB up to 1 GHz.

D. Signal Sampling With the Sensor

The acquired samples form a set of measurements of a random variable. Determining the probability distribution of the measured signal and extracting its statistical characteristics, such as mean, peak-to-peak amplitude, standard deviation, etc., provide valuable information. A histogram is an adapted graphical representation of a probability distribution.

However, it provides only an estimation of the actual probability distribution of the measured signal. The accuracy depends on both the number of samples and the number of bins (i.e., a discrete interval of the measured signal range) which has to be carefully chosen. A small number of bins reduces the resolution of the histogram and degrades the accuracy of the

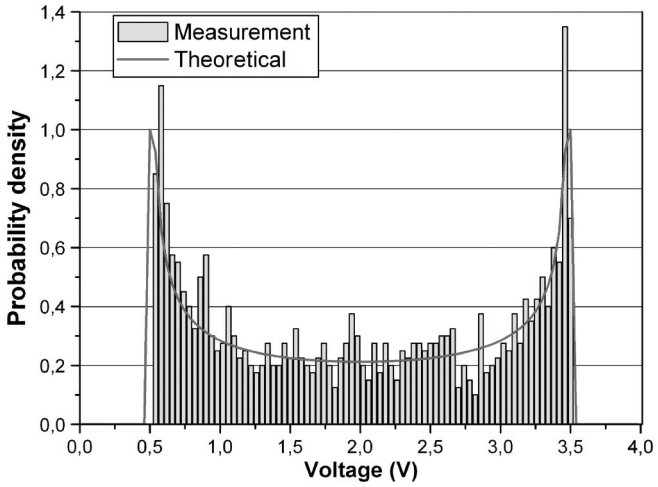

Fig. 8. Measured and theoretical pdfs of a sinusoidal signal.

extraction of statistical properties, while a too large number of bins increases the number of spikes on the histogram. Several theoretical works have attempted to provide algorithms [20] or formulas to find an optimal number of bins N from the number of samples n, such as Sicard–Max or Sturge formula [21]

$$N = 1 + \log_2(n) = 1 + 3.3.\log_{10}(n). \tag{3}$$

A usual choice of bin number is given by the square root choice given by

$$N = \sqrt{n}. \tag{4}$$

However, all of these formulas suffer from the assumption made on the type of distribution and the large number of samples. Therefore, the number of bins can be experimentally set to optimize the number of samples and the histogram resolution. A rule of thumb is to ensure that the bin width remains larger than the measurement resolution. Experimental results have shown that the sensor resolution is about 10 mV.

In order to verify the correctness of probability distribution extracted from sensor measurement, the pdf of a basic signal is measured with the on-chip sensor. Fig. 8 shows the histogram obtained with a sinusoidal signal. The signal frequency is set to 10 MHz, and its peak-to-peak amplitude is equal to 3 V. The signal is randomly sampled 2000 times at 50 kHz. The number of bins is set to 100, and the bin width is equal to 37.5 mV. As shown in Fig. 8, the sensor measurement result is in accordance with the theoretical pdf given by

$$p(x) = \frac{1}{\pi\sqrt{1-x^2}}, \qquad |x| < 1. \tag{5}$$

V. Study of Digital core Susceptibility With the On-Chip Noise Sensor

The on-chip noise sensor is now used to study the susceptibility of a digital core to conducted interferences coupled on its power supply. Sensor measurements aim at determining the amount of voltage fluctuations induced on the core power supply internally, characterizing the actual susceptibility level of the digital core and understanding the failure mechanism.

A. Case Study and Experimental Setup Description

An LV-range on-chip noise sensor (0–3.75 V) has been placed along the power supply rail of a digital core, in order to measure the amplitude and the statistical distribution of EMI-induced voltage fluctuations. The digital core is composed of a string of buffers which delays an input signal and is terminated by an edge-triggered D flip-flop synchronized by a clock signal. The core is supplied by a dedicated and decoupled 2.5-V power supply. Core I/Os are made of two parts: a level shifter powered by the 2.5-V core power supply and the I/O buffer powered by a dedicated 5-V power supply.

Harmonic disturbances are injected on the digital core power supply pin according to the DPI standard over the range of 1–1000 MHz. The experimental test bench is described in Fig. 9.

The circuit, mounted in a 128 TQFP package, is soldered on a four-layer EMC test board. The 2.5- and 5-V power planes are carefully decoupled and isolated from DPI injection points by choke inductances. During the susceptibility tests, two types of experiments are performed. First, the EMI-induced noise on the core power supply is measured for a constant level of conducted disturbance. The EMI-coupling transfer function, i.e., the ratio between the amplitude of voltage fluctuations and the forward power of the conducted disturbance, can be extracted. In order to demonstrate the relevance of on-chip noise measurements, the EMI-transfer function is extracted by the following.

1) Off-chip measurement: The EMI-induced noise is measured across the core power supply package pin by a 2-GHz digital oscilloscope equipped with a 2.5-GHz active probe.
2) On-chip measurement: The EMI-induced noise is measured internally along the core power supply rail pin by the on-chip noise sensor.

The second experiment consists in correlating core failures induced by conducted interferences with the voltage fluctuations measured by the on-chip noise sensor. Core failures are associated to binary errors and are detected by monitoring the core output signal in the time domain. Two failure criteria are defined to detect core failures.

1) A degradation of the logic level amplitude due to noise coupling. As the required power to induce a change of the logic state of the output signal is very large, we set the maximum allowed noise amplitude to 10% of the nominal power supply (i.e., 0.5 V).
2) A shift of one-half of the clock period (i.e., $\pm$50 ns) of the arrival time of output logic state due to EMI-induced jitter.

B. Off-Chip and On-Chip EMI-Induced Noise Measurements

In order to compare the off-chip and on-chip EMI-coupling transfer functions, the forward power of the conducted interference is measured each time that on-chip and off-chip voltage fluctuations exceed a given voltage value. This voltage value is

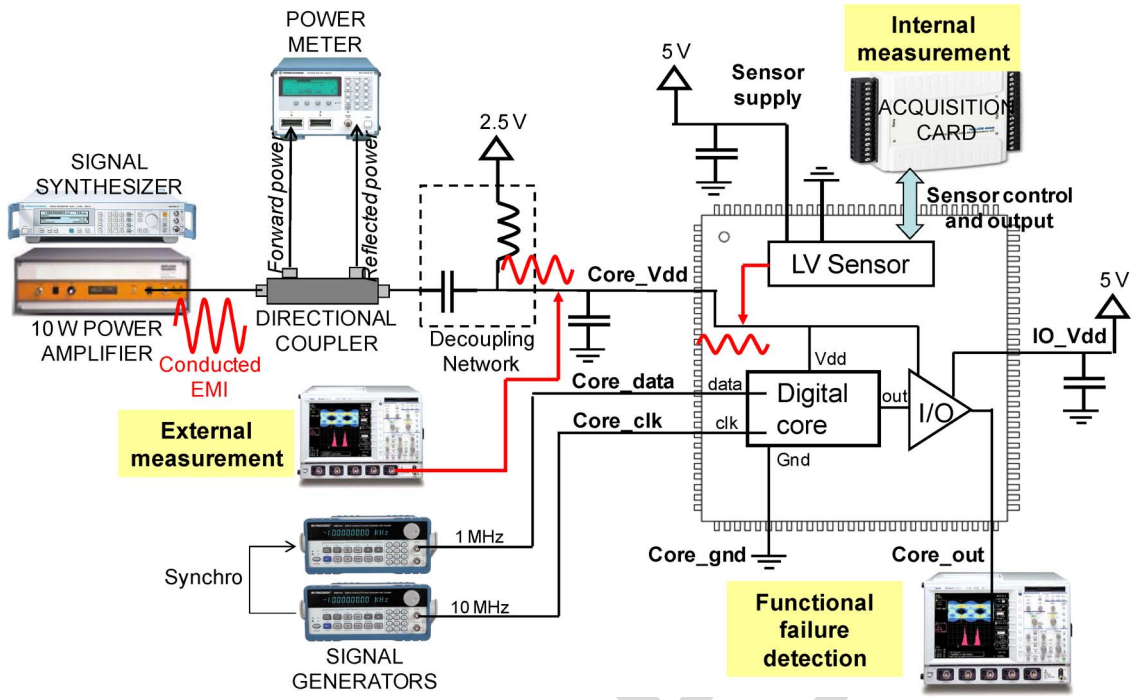

Fig. 9. Experimental setup for the characterization of the conducted susceptibility of the digital core.

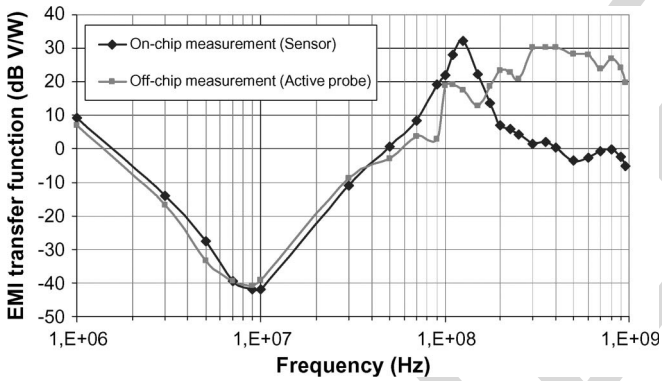

Fig. 10. Comparison of off-chip and on-chip EMI-coupling transfer functions.

set to 0.25 V to ensure a small-signal condition. As harmonic disturbances are injected, this condition can be checked by measuring the symmetry of the pdf of voltage fluctuations.

Fig. 10 shows the comparison of off-chip and on-chip EMI-coupling transfer functions. Below 50 MHz, both measurement methods provide identical results. Off-chip and on-chip voltage fluctuations are identical. Around 10 MHz, the weakness of EMI coupling is explained by the efficiency of the test board decoupling. However, above 50 MHz, both measurement methods give different results. Between 50 and 200 MHz, the on-chip measured EMI-induced noise is larger than that of the off-chip noise. The on-chip EMI coupling is optimized at 140 MHz. Above 140 MHz, the on-chip EMI coupling decreases, and the off-chip noise measurement exceeds the on-chip noise one.

As the cutoff frequencies of both measurement systems exceed 1 GHz, the observed differences cannot be explained by their frequency limits but by the differences in measurement locations. The significant measurement discrepancies between the on-chip and the off-chip EMI-induced noise can lead to different evaluations of circuit susceptibility. These measurements show that the on-chip noise sensor provides a more accurate measurement of EMI coupling across the digital core above 50 MHz. Around 100 MHz, the amount of EMI-induced noise tends to be underestimated by off-chip measurements, while it is overestimated above 200 MHz. Moreover, the complex on-chip propagation of conducted EMI can be understood more clearly by on-chip noise sensor measurements.

C. Analysis of EMI Coupling on Core Power Supply

In order to clarify the origins of differences between off-chip and on-chip measurements, an electrical model of the circuit including the package, the EMC test board, and the DPI test bench has been built. The central part of the model is formed by the PDN of the core. The main elements of the PDN are the physical interconnects of the core power supply rails, the equivalent capacitance of the core, and the I/O pads. An *RC* extraction tool is used to extract the core equivalent capacitance and interconnect resistance. Package pins add parasitic inductances to the core PDN, which can be computed by quasi-static approximations from the package geometrical dimensions.

However, although the power supply domains of the different blocks of the circuit are separated, they can interact due to parasitic couplings. Onboard measurements of EMI propagation between 5- and 2.5-V power planes have shown that parasitic couplings at board level are negligible. At circuit level, two coupling mechanisms predominate. First, as the different blocks of the circuit share the same P^+ substrate, a significant substrate coupling exists between the ground connections of each block. Impedance measurements are performed to extract the resistive network which interconnects the ground connections of the different blocks of the circuit. Second, the core and the I/O

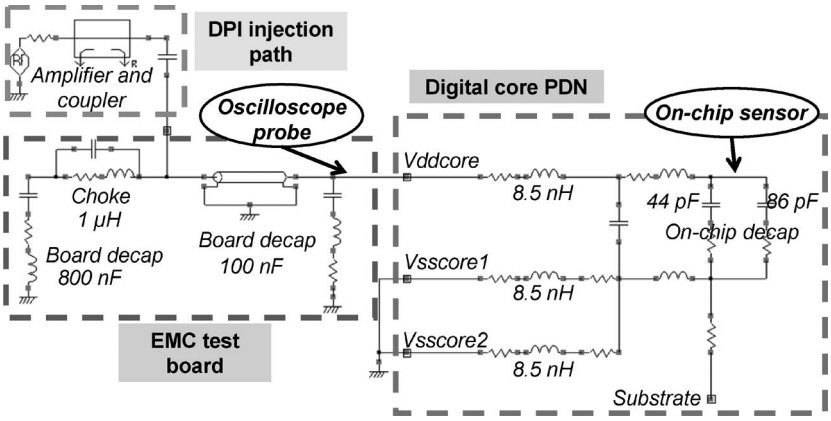

Fig. 11. Model of the digital core PDN including the EMC test board and the DPI injection.

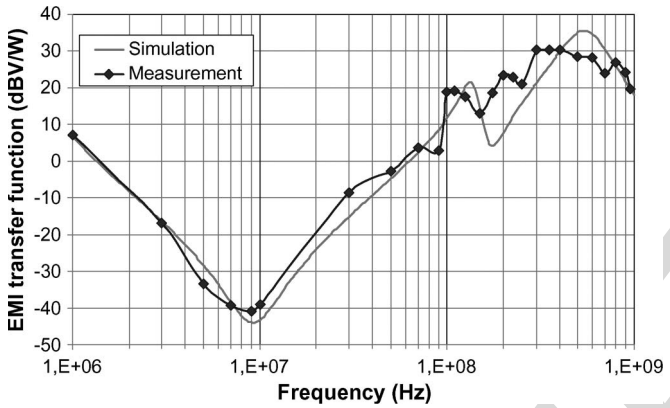

Fig. 12. Comparison between measurement and simulation of off-chip EMI-coupling transfer function.

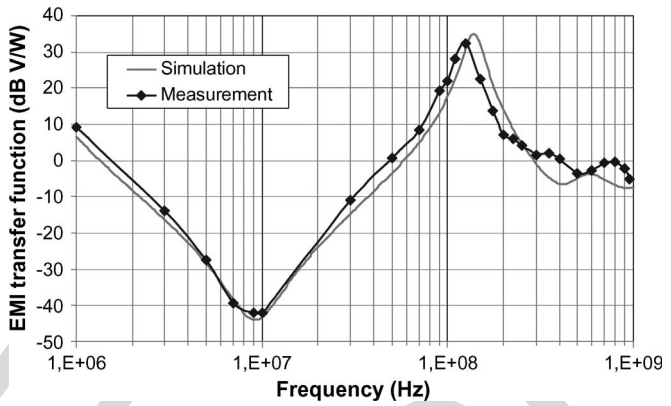

Fig. 13. Comparison between measurement and simulation of on-chip EMI-coupling transfer function.

power supplies are coupled by parasitic capacitors through the ESD protections of core power supply pads. These parasitic capacitors can be estimated by RC extraction.

Finally, S parameter measurements between the different pins of the core PDN are done with high-frequency probes in order to validate the circuit model. A simplified version of the final model is shown in Fig. 11. Positions of voltage probes to extract the off-chip and the on-chip EMI-induced noise are indicated. IC-EMC software [22] is used to perform ac simulations and compute the EMI-coupling transfer functions.

The comparisons between measured and simulated off-chip and on-chip EMI-coupling transfer functions are presented in Figs. 12 and 13, respectively.

The good agreement between simulation and measurement curves validates the circuit model. The slight differences between measurements and simulations are mainly due not only to measurement uncertainties but also to inaccuracies in models of external passive devices, package interconnects, and substrate coupling. The analysis by simulation of the core electrical model helps us to understand the difference between off-chip and on-chip EMI couplings. The circuit package, IC interconnects, and equivalent on-chip capacitance act as a low-pass filter above 50 MHz. The on-chip EMI-coupling optimum measured at 140 MHz is due to the resonance between package inductances and core equivalent capacitance. Above the resonance frequency, the on-chip decoupling filters EMI-induced voltage fluctuations efficiently.

D. Analysis of Core Failure by On-Chip Sensor Measurements

The second part of the experiment aims at correlating the core failures induced by conducted disturbances with sensor measurement to verify the responsibility of the core for failures and determining its sensitivity level to EMI-induced noise. First, the susceptibility level of the core is measured according to the DPI test setup described in Fig. 9. Fig. 14 shows the amount of forward power of the conducted harmonic disturbance to induce a core failure. The power amplifier can deliver up to 40 dBm without saturation. Two types of failures arise: either timing jitter on the core output signal or a degradation of logic levels due to an excessive noise. For each test frequency, the type of failure is pointed out on the curve. Below several megahertz, conducted disturbances lead to a significant timing jitter, while they disturb output signal logic levels above several tens of megahertz.

The susceptibility threshold can be compared to the on-chip EMI transfer function (Fig. 13). The circuit sensitivity to EMI is very weak between 2 and 50 MHz because the coupling of EMI is not efficient over this frequency range due to board decoupling. As the EMI coupling on the core power supply node is the most efficient at 140 MHz, we can expect a marked sensitivity of the circuit around this frequency. Although a susceptibility peak appears at 140 MHz, the circuit is the more sensitive at 500 and 950 MHz. Above 200 MHz, the

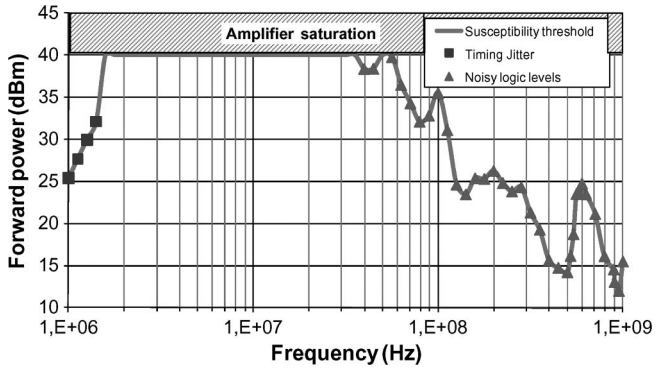

Fig. 14. Measurement of the susceptibility threshold of the digital core.

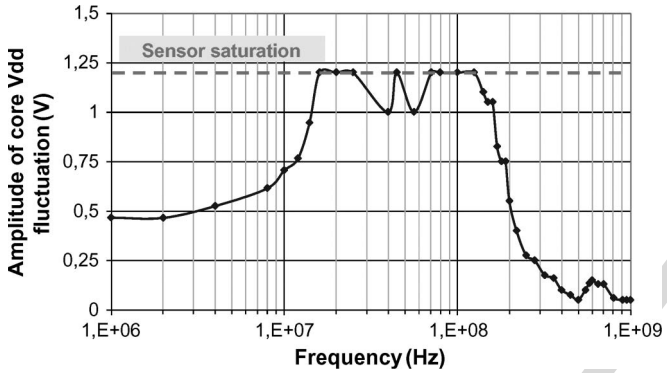

Fig. 15. Measurement of the amplitude of digital core power supply voltage fluctuation at failure occurrence.

susceptibility of the core no longer seems correlated to power supply voltage fluctuations.

The on-chip noise sensor is used to correlate failure occurrences and the amount of noise induced on core power supply. At each disturbance frequency, the amplitude of the core power supply voltage fluctuation is picked up when a failure arises or when the power amplifier saturates, and is reported on the graph in Fig. 15. As the nominal core power supply is equal to 2.5 V and the LV sensor range is limited to 3.75 V, the sensor output saturates when the voltage fluctuation amplitude exceeds 1.2 V.

On-chip noise sensor measurement shows that the core failures are strongly linked to core power supply voltage fluctuations up to 160 MHz. Below 10 MHz, the circuit is very sensitive to core power supply voltage fluctuations which induce timing jitter on the output signal. The sensitivity level of the core tends to decrease at higher frequency. As explained in [23], the amount of EMI-induced jitter which affects digital gates is not only proportional to the EMI amplitude but also frequency dependent. For a constant level of EMI, the induced jitter tends to reduce when the frequency increases. Between 20 and 160 MHz, failure occurs for a nearly constant level of voltage fluctuation, very close to the saturation level of the sensor. When the core power supply ripple exceeds 1.25 V (half of the core power supply voltage), the core operation is strongly affected, and the output signal logic levels starts to be altered.

However, above 160 MHz, failures happen without significant core power supply voltage fluctuations. The degradation of the output signal can no longer be explained by the disturbance of the core operation, but it seems to be linked to a direct disturbance of the output buffer. The failure mechanism of the digital core to conducted interferences along the core power supply includes not only the core but also the output buffer. This hypothesis about the origin of the failure is studied with an additional on-chip sensor measurement in the following part.

E. Analysis of I/O Failure by On-Chip Sensor Measurements

Although core and I/O supply domains are separated, they are connected by ESD protections and coupled by parasitic capacitances associated to ESD protections and core power supply pads. A sensor placed on the output buffer power supply could confirm the hypothesis of a noise coupling between core and output buffer power supplies, but unfortunately, it has not been planned at test chip specification. However, a similar I/O has been isolated with 2.5- and 5-V power supplies for the level shifter and the output buffer, respectively. An MV-range on-chip sensor has been placed on the output buffer power supply to monitor voltage fluctuations.

This sensor can be used during conducted injection on the 2.5-V power supply of the level shifter to have a qualitative evaluation of the impact of the parasitic coupling between core and output buffer power supplies. This measurement done on the isolated I/O block does not give us directly the exact level of coupling between digital core and output buffer since I/O and digital core blocks have different PDNs. However, we can expect to observe similar effects because the PDN structure is the same for both blocks. The proposed measurement aims at highlighting a possible significant coupling between digital core and output buffer power supplies and detecting a frequency range where the output buffer power supply is disturbed by the conducted injection done on core power supply.

A DPI injection is performed on the level shifter power supply of the isolated I/O. Only failures associated to a degradation of the logic level amplitude of the output signal appear. When a failure arises (if the noise amplitude on the output signal exceeds 0.5 V), the amplitude of the noise induced on the output buffer power supply is measured with the on-chip sensor. The experimental test bench is shown in Fig. 16.

The sensor measurement of the noise coupled on the output buffer power supply is shown in Fig. 17. The voltage fluctuation remains negligible when a failure arises below 100 MHz, so the noise measured on the output signal is not related to the output buffer power supply voltage fluctuation but to that of the level shifter power supply. The comparison with sensor measurement on core power supply shows that the failure is only linked to the core, not to the output buffer. However, the noise coupled on the output buffer power supply becomes very significant between 100 and 450 MHz. Moreover, it becomes large enough to trigger ESD protections between both power supply domains and corrupt the logic level of the output signal. Over this range, the I/O failure is due to the coupling of conducted noise on the output buffer power supply which disturbs the output buffer operation. The increase of the output buffer power supply voltage fluctuation can be compared to the reduction of that of

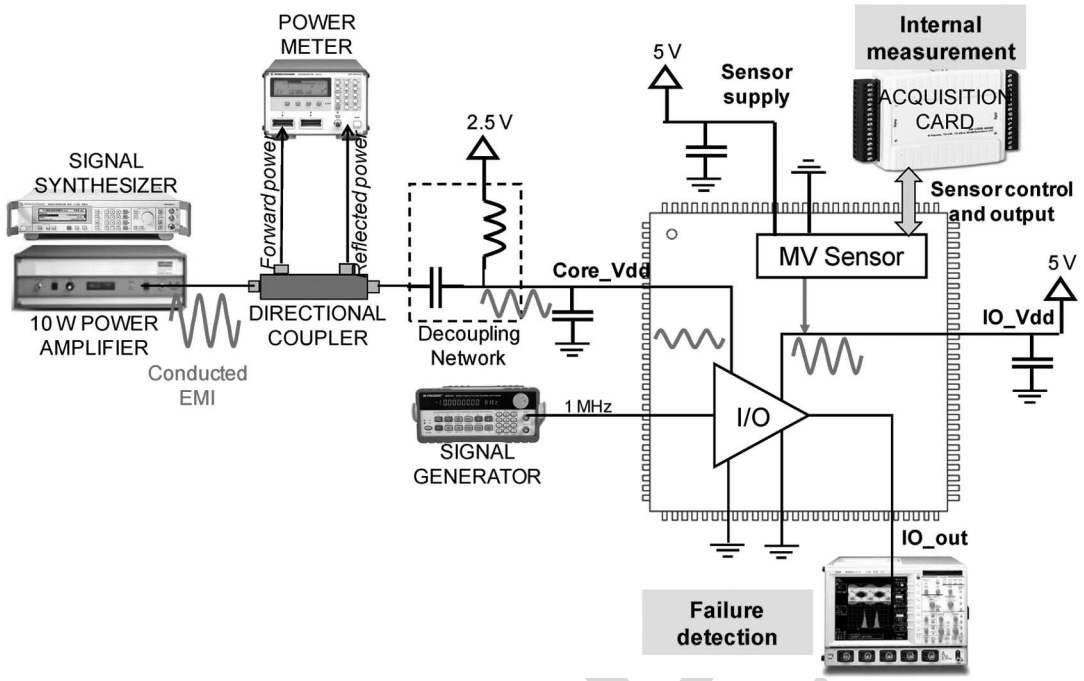

Fig. 16. Experimental setup for the characterization of the coupling between core and I/O power supplies.

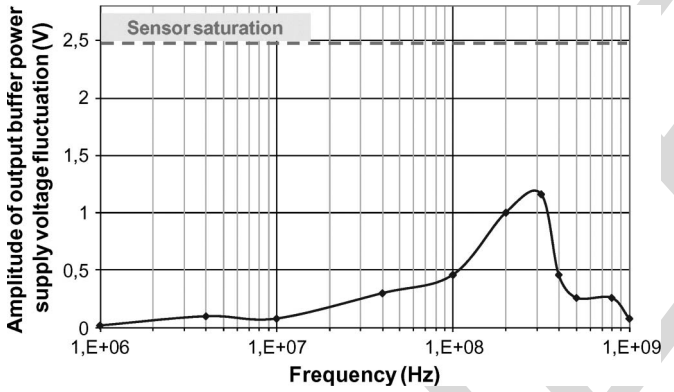

Fig. 17. Measurement of the amplitude of output buffer power supply voltage fluctuation at failure occurrence.

the core power supply over the same frequency range (Fig. 15). The combination of on-chip noise measurement on core and output buffer power supplies confirms that the output buffer has a significant impact on the digital core failure mechanism.

Above 450 MHz, the noise amplitude on the output buffer power supply is reduced. The I/O failure seems to be no longer associated to output buffer power supply fluctuations. The on-chip sensor measurements on core and output buffer power supplies fail to provide a satisfactory explanation of the digital core failure mechanism above 450 MHz. The coupling of EMI on other nodes of the circuit is responsible of the observed failures. For example, the output node of the core is strongly affected by EMI-induced noise, externally coupled through the PCB. Experimental observations show that, above a certain amplitude, the noise on the output signal is able to trigger ESD protections. A more accurate understanding of the core failure could be obtained by placing a larger number of sensors over the digital core, particularly on the core output node.

VI. Conclusion

This paper has presented an on-chip sensor dedicated to the characterization of circuit susceptibility, based on a random subsampling of voltage fluctuations across sensitive nodes. Although this acquisition mode does not allow a reconstruction of signal waveform in time domain, the amplitude of EMI-induced voltage fluctuations and signal distortions can be extracted without complex experimental setup and postprocessing. Several versions of this sensor have been developed in 0.25-μm CMOS process for various voltage ranges. The main advantages of this sensor are its small surface, its large bandwidth (up to 2 GHz in the LV range), its high linearity, and robustness to electrical stress, at the price of a simple design.

This sensor has been used to study the susceptibility of a digital core to conducted disturbances. On-chip sensor measurements offer a more accurate evaluation of EMI-induced noise than off-chip measurements above several tens of megahertz because of the package and circuit filtering effect. For circuit designers, using this type of on-chip sensor is of great interest because it provides a precise characterization of noise propagation within the die and helps to identify the sensitive blocks, extract their actual susceptibility level, and validate their models. Placing a network of such a sensor on each sensitive node of a circuit (e.g., power supply and ground rails, sensitive input, reference voltage, etc.) could facilitate failure diagnosis and the modeling of complex parasitic couplings between separated blocks, such as substrate coupling, crosstalk, etc.

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